Solution ID: rd05162013_635
Last Modified: Jun 03, 2013
Product Category: Design Software
Product Area: Project Management/Scripting
Product Sub-area: Tcl/QSF/SDC
Version Found In: v8.0
Software: Quartus II Linux,Quartus II PC

Title

How do I embed timing constraints in my HDL file?

Description

Timing constraints in Synopsys Design Constraint (SDC) format can be embedded in VHDL or Verilog HDL design files when using Quartus® II synthesis. Use the `altera_attribute` keyword in your HDL file to and the `SDC_STATEMENT` option to apply a timing constraint. Note that only one `altera_attribute` is allowed per VHDL entity or Verilog HDL module. To apply multiple constraints combine all options or assignments into one line, separating each with a semicolon (;).

Below is an example of applying multiple false-path timing constraints using the `altera_attribute` keyword and the `SDC_STATEMENT` otpion in Verilog-2001 HDL format. For other HDL language formats, refer to **Using `altera_attribute` to Set Quartus II Logic Options** in the *Quartus II Integrated Synthesis* (PDF) chapter of the Quartus II Handbook.

```
(* altera_attribute = {"-name SDC_STATEMENT \"set_false_path -from
[get_registers *sv_xcvr_pipe_native*] -to [get_registers *altpcie_rs_serdes|*]
\";-name SDC_STATEMENT \"set_false_path -to [get_registers
*altpcie_rs_serdes|fifo_err_sync_r\[0\]]\";-name SDC_STATEMENT \"set_false_path
-to [get_registers *altpcie_rs_serdes|busy_altgxb_reconfig*]\""} *)
```

Feedback

This solution answers my question: Strongly Disagree 1 2 3 4 5 Strongly Agree

This solution was easy to find: Strongly Disagree 1 2 3 4 5 Strongly Agree

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