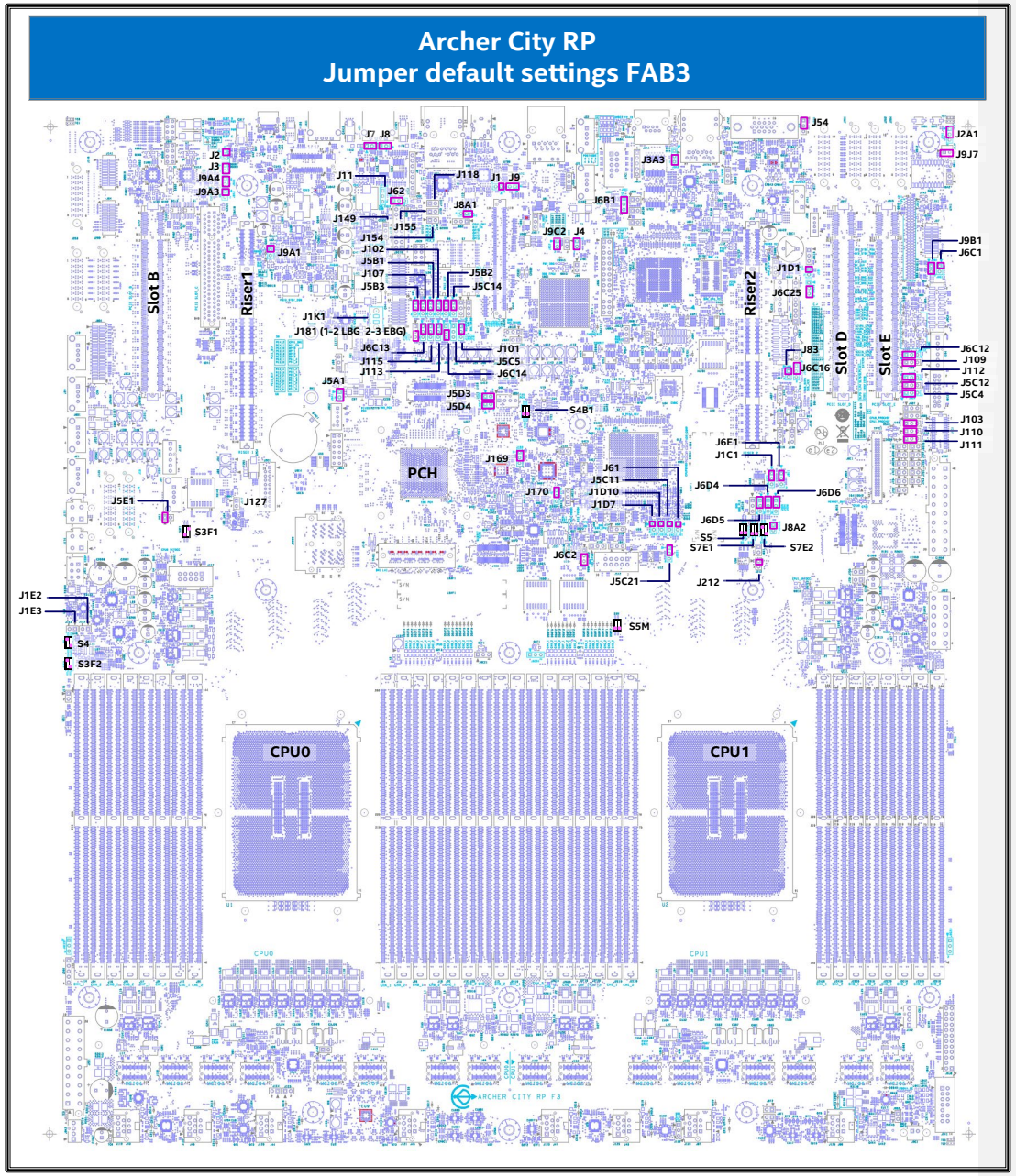
Archer City Reference Platform (RP) Jumper Settings

Archer City Bring Up Recipe

- Default Jumper/Switch settings:
  - Always remember to check Jumper settings. This is a **critical** (and often skipped) step to successfully turning a platform on.
  - Make sure your settings meet the platform's default settings or the one you require for your specific configuration.



CPU Jumpers

Ref Des	Default	Description
J5D3	1-2	**CPU0 JTAG bypass** 1 Bypass CPU0 1-2 Normal operation
J5D4	1-2	**CPU1 JTAG bypass** 1 Bypass CPU1 1-2 Normal operation
J8A1	1	**Socket Occupied CPU0** 1 Disabled 1-2 Enabled
J8A2	1	**Socket Occupied CPU1** 1- Disabled 1-2 Enabled
J9A3	1	**Hotplug Slot B MRL** 1-2 after card is connected 1 before card is removed
J9A4	1-2	**Hotplug Slot B force voltage** 1-2 to force all PCIe voltage rails 1 to support hotplug.
J9C2	1-2	**Hotplug Slot B** 1-2 Disabled 1 Enabled
J6C2	2-3	**BMCINIT** 1-2 High 2-3 Low (Normal boot flow)
S3F1.1	OFF	**Safe boot mode CPU0** ON: Enable OFF: Disabled
S3F1.2	ON	**TXT Agent CPU0** ON: CPU is TXTagent OFF: CPU isn't TXTagent
S3F2.1	ON	**BIST Enabled CPU0** ON: Disabled OFF: Enabled
S3F2.2	OFF	**TXT Platform enabled CPU0** ON: Disabled OFF: Enabled
S7E1.1	OFF	**Safe boot mode CPU1** ON: Enabled OFF: Disabled
S7E1.2	OFF	**TXT Agent CPU1** ON: CPU is TXTagent OFF: CPU isn't TXTagent
S7E2.1	ON	**BIST Enabled CPU1** ON: Disabled OFF: Enabled
S7E2.2	OFF	**TXT Platform enabled CPU1** ON: Disabled OFF: Enabled
S4.1	ON	**Boot Mode strap (SPR & GNR)** ON: PCH boot mode OFF: CPU boot mode
S4.2	OFF	**GPIO 4: Boot Mode (SPR & GNR)** ON: CPU boot mode OFF: PCH boot mode
S5M.1	OFF	**Die HVM En CPU0** ON: Only master die OFF: Normal operation
S5M.2	OFF	**Die HVM En CPU1** ON: Only master die OFF: Normal operation

PCH Jumpers (1/2)

Ref Des	Default	Description
J2	1	**Hotplug Slot C MRL** 1-2 after card is connected 1 before card is removed.
J3	1-2	**Hotplug Slot C force voltage** 1-2 to force all PCIe voltage rails 1 to support hotplug.
J9A1	1	**Force SLP SUS** 1-2 Turn on Platform without PCH. Only manufacturing test.
J62	1-2	**SPI Voltage** 1-2 SPI 3.3V 2-3 SPI 1.8V Remove jumper to use Dediprog.
J6B1	1-2	**eSPI CS0# flow (eSPI mode)** 1-2 CS0# to BMC 2-3 CS0# to LPC/eSPI conn
J4	1-2	**Hotplug Slot C** 1-2 Disabled 1 Enabled
J102	1-2	**VISA** 1-2 Native function enable 2-3 VISA Enable
J5B1	1-2	**LT KEY downgrade** 1-2 Disabled 2-3 Enabled
J107	1-2	**DFX Test Mode** 1-2 Disabled 2-3 Enabled
J5B3	1-2	**BIOS image swap** 1-2 Normal 2-3 Enable Bios image Swap
J1K1	empty	**MFG JUMPER**
J6C13	1-2	**Password clear** 1-2 Normal 2-3 Password clear
J115	1-2	**SPI Voltage buffer on EBG** 1-2 SPI 3.3V 2-3 SPI 1.8V
J5A1	1-2	**Battery removed** 1-2 Battery connected 1 Battery disconnected
J113	1-2	**eSPI CS Swizzle** 1-2 CS0 and CS1 pins have the default assigment 2-3 CS0 and CS1 are swizzled
J6C14	3	**ME FW Update** **LBG N-1:** 1-2 Don't allowed 2-3 ME Force Update 3 Normal **EBG:** 1-2 Normal 2-3 ME Force Update

PCH Jumpers (2/2)

Ref Des	Default	Description
J5C5	1-2	**eSPI or LPC** 1-2 eSPI 2-3 LPC
J101	1-2	**eSPI strap** 1-2 eSPI is enabled 2-3 eSPI is disabled
J5C14	1-2	**Flash security override** 1-2 Disabled 2-3 Enabled
J5B2	1-2	**Bios swap override** 1-2 Disabled 2-3 Enabled
J6C12	1-2	**BIOS advance functions** 1-2 Normal 2-3 Bios core execution tree
J5C4	1-2	**Bios Recovery mode** 1-2 Normal 2-3 Recover Bios
J112	1-2	**JTAG ODT** 1-2 JTAG ODT enabled 2-3 JTAG ODT disable
J5C4	1-2	**BIOS recovery mode** 1-2 Normal 2-3 Recovery mode
J103	1-2	**IO Expander mode** 1-2 PCH mode (Default) 2-3 Recovery mode
J111	1-2	**Xtal Selection** 1-2 25 MHz (Default) 2-3 100 MHz
J110	1-2	**External clock mode** 1-2 Diff. input buffer 2-3 Xtal Amp mode
J109	1-2	**LAN enable** 1-2 ON 2-3 OFF
J5E1	1	**RST TPM** 1 Enable TPM 1-2 Keep TPM on reset
J5C12	1-2	**No reboot strap** 1-2 Enabled 2-3 Disabled
J181	2-3	**PVNN Vout** 1-2 Vout = 0.9v (LBG & EBG B0) 2-3 Vout = 1.05v (EBG A0)
J2A1	1-2	**CMOS clear** 1-2 Normal RTC rst 2-3 Clear RTC registers
S4B1	open - open	**CPU interposer type selection (CPU0 + CPU1)** S4B1.1 & S4B1.2 OPEN / OPEN -> A + A OPEN / CLOSE -> A + B CLOSE / OPEN -> B + A CLOSE / CLOSE -> B + B

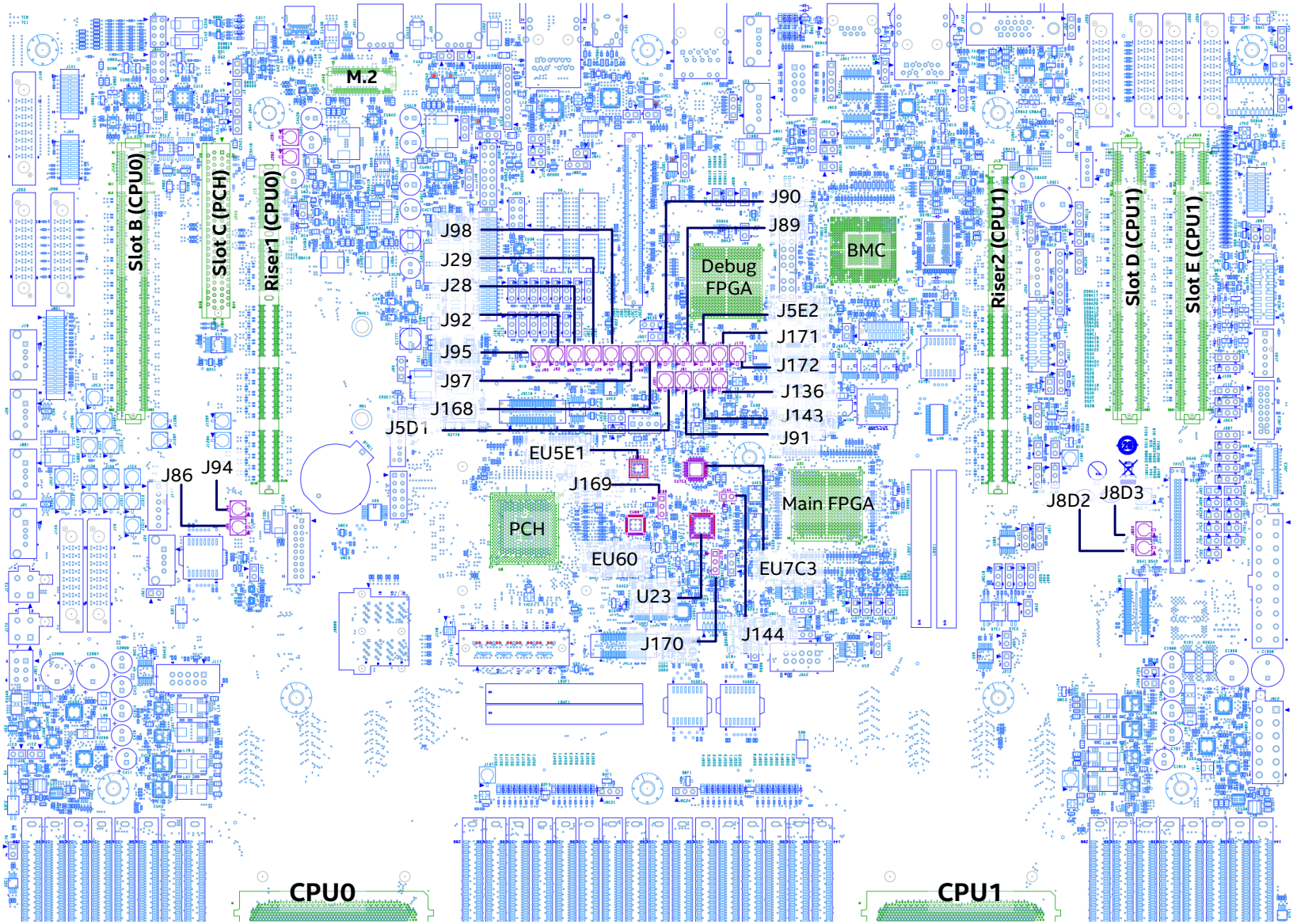
FPGA Jumpers		
Ref Des	Default	Description
J9B1	1-2	**PS_PWRGD to the system** 1 Disconnected 1-2 connected
J1D10	1	**PERST_N options bit0** 1-2 PLTRRST_N 1 CPU PWRGD
J1D7	1	**PERST_N options bit1** 1-2 PLTRRST_N 1 CPU PWRGD
J1D1	1	**PERST_N options bit2** 1-2 PLTRRST_N 1 CPU PWRGD
J5C11	1	**ADR ext trigger** 1 Normal operation 1-2 ADR ext triggered
J61	1	**FAN FPGA enabled** 1 BMC contolrs fans 1-2 FPGA controls fans
J6D6	1-2	**PRF T-1 hold** 1-2 Normal 2-3 Force PFR hold
J6D4	1-2	**PFR postcode** 1-2 Normal operation 2-3 PFR postcodes mode
J6D5	1-2	**PFR force recovery** 1-2 Normal operation 2-3 Force PFR recovery
J6E1	1-2	**FPGA programming enabled** 1-2 Enabled 2-3 Disabled
J1C1	1-2	**Force PWRON** 1-2 Disable 2-3 Enable

SMBUS Jumpers		
Ref Des	Default	Description
J7	1-2	Remove jumper to attach SMB_TEMP_SENSOR to SMLINK3.
J8	1-2	Remove jumper to attach SMB_PCIe to SMLINK3.
J1	1	Remove jumper to attach SMB_LAN to SMLINK3.
J9	1-2	Remove jumper to attach SMB_LAN to SMLINK0. Don't use at same time as J1.
J212	1	1-2 Isolate PMBUS

BMC Jumpers		
Ref Des	**Default**	**Description**
J3A3	2-3	**DCD/DSR to DTR** 1-2 DCD to DTR 2-3 DSR to DTR
J6C25	2-3	**BMC Remote Debug** 1-2 Enable 2-3 Disable
J6C1	1	**Force BMC update** 1 Normal 1-2 Force BMC Update
J6C16	1-2	**PECI Master** 1-2 BMC is master 2-3 PCH is master
J5C21	1-2	**BMC SPD remtome debug** 1-2 Disabled 2-3 Enabled
J54	1-2	**EMMC PFR enable** 1-2 Enabled 2-3 Disabled

CLK Jumpers		
Ref Des	**Default**	**Description**
J169	1-2	**Spread Spectrum** 1-2 Enabled 2-3 Disabled
J170	1-2	**Clock Spread** **1** Low spread **1-2** High spread -0.5% **2-3** VDD/2Spread -0.3%

Interposer Jumpers		
Ref Des	**Default**	**Description**
S4B1	open - open	CPU interposer type selection (CPU0 + CPU1) S4B1.1 & S4B1.2 OPEN / OPEN -> A + A OPEN / CLOSE -> A + B CLOSE / OPEN -> B + A CLOSE / CLOSE -> B + B
S5	close	S5.2 OPEN -> SPR CLOSE -> CPU interposer used (CLX or BRS)



CLK SMA connectors	
Ref Des	**Description**
J94	PCH iSCLK test (CLK out7 DP)
J86	PCH iSCLK test (CLK out7 DN)
J98	External 100MHz injection for EU5E1 (DP)
J97	External 100MHz injection for EU5E1 (DN)
J28	External 25MHz injection for EBG (DP)
J29	External 25MHz injection for EBG (DN)
J92	32.76KHz RTC XTAL EBG test (RTCX1)
J168	Si5332 25Mhz XTAL test (XTAL_SI5332_IN)
J5D1	CK440 PFT IN injection (DP)
J91	CK440 PFT IN injection (Dn)
J89	CK440 PFT OUT test (DP)
J90	CK440 PFT OUT test (DP)
J5E2	25MHz XTAL CK440 test (XIN)
J172	CK440 100MHz test (CLK out 2 DP)
J171	CK440 100MHz test (CLK out 2 DN)
J143	CK440 MXCLK test (CLK out 2 DP)
J136	CK440 MXCLK test (CLK out 2 DN)
J8D3	100MHz CLK LAI test (DP)
J8D2	100MHz CLK LAI test (DN)

CLKs	
Ref Des	**Description**
EU5E1	CLK buffer DB2001 Outs: Risers, SlotB, SlotD, SlotE, BCKLs CPU
EU9	CLK buffer DB2001 Outs: NVMEs
EU60	CLK generator SI5332
U23	CLK generator CK440
EU7C3	CLK generator CKMNG

Board SMBus Jumpers

J5C17	HOST
J5C19	SMLINK1
J5C20	SMLINK2
J11	SMLINK3
J5C18	PMBUS 1
J149	PMBUS 2
J6C19	PMBUS3
J2A2	PCIe STBY
J6C26	TEMP SENSORS
J6C16	PECI
J3A5	LAN
J6C21	CPU0 SPD DDR5 ABCD
J6C22	CPU0 SPD DDR5 EFGH
J6C23	CPU1 SPD DDR5 ABCD
J6C24	CPU1 SPD DDR5 EFGH