MINGW64:/c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/software

```
bash: /c/intelFPGA_pro/20.1/embedded/host_tools/altera/ds5_link/soceds_config: N
o such file or directory
WARNING: DS-5 install not detected. SoC EDS may not function correctly without a
 DS-5 install.
-----------------------------------------------
Intel FPGA Embedded Command Shell

Version 20.1 [Build 177]
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3O5O19592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded
$ quartus_pgm -c 1 -m jtag -o "p;$SOCEDS_DEST_ROOT/examples/hardware/a10_soc_devkit_ghrd/output_files/ghrd_10as066n2.sof"
Info: *******************************************************************
Info: Running Quartus Prime Programmer
    Info: Version 20.1.0 Build 177 04/06/2020 SC Pro Edition
    Info: Copyright (C) 2020  Intel Corporation. All rights reserved.
    Info: Your use of Intel Corporation's design tools, logic functions
    Info: and other software and tools, and any partner logic
    Info: functions, and any output files from any of the foregoing
    Info: (including device programming or simulation files), and any
    Info: associated documentation or information are expressly subject
    Info: to the terms and conditions of the Intel Program License
    Info: Subscription Agreement, the Intel Quartus Prime License Agreement,
    Info: the Intel FPGA IP License Agreement, or other applicable license
    Info: agreement, including, without limitation, that your use is for
    Info: the sole purpose of programming logic devices manufactured by
    Info: Intel and sold by Intel or its authorized distributors.  Please
    Info: refer to the applicable agreement for further details, at
    Info: https://fpgasoftware.intel.com/eula.
    Info: Processing started: Tue Jul 26 13:50:06 2022
    Info: System process ID: 16604
Info: Command: quartus_pgm -c 1 -m jtag -o p;C:/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/output_files/ghrd_10as066n2.sof
Info (213045): Using programming cable "USB-BlasterII [USB-1]"
Info (213011): Using programming file C:/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/output_files/ghrd_10as066n2.sof with checksum 0x1CB34383 for device 10AS066N3F40@1
Info (209060): Started Programmer operation at Tue Jul 26 13:50:10 2022
Info (209016): Configuring device index 1
Info (209017): Device 1 contains JTAG ID code 0x02E050DD
Info (209007): Configuration succeeded -- 1 device(s) configured
Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Tue Jul 26 13:50:22 2022
Info: Quartus Prime Programmer was successful. 0 errors, 0 warnings
    Info: Peak virtual memory: 1167 megabytes
    Info: Processing ended: Tue Jul 26 13:50:22 2022
    Info: Elapsed time: 00:00:16
    Info: System process ID: 16604

3O5O19592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded
$ cd $SOCEDS_DEST_ROOT/examples/hardware/a10_soc_devkit_ghrd/

3O5O19592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd
$ rm -rf software/bootloader

3O5O19592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd
$ mkdir -p software/bootloader

3O5O19592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd
$ cd software/bootloader

3O5O19592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/software/bootloader
$ git clone https://github.com/altera-opensource/u-boot-socfpga
Cloning into 'u-boot-socfpga'...
fatal: unable to access 'https://github.com/altera-opensource/u-boot-socfpga/': Could not resolve host: github.com

3O5O19592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/software/bootloader
$ export https_proxy=3.87.248.1:88
```

```
3O5019592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/software/bootloader
$ git clone https://github.com/altera-opensource/u-boot-socfpga
Cloning into 'u-boot-socfpga'...
remote: Enumerating objects: 860036, done.
remote: Counting objects: 100% (58086/58086), done.
remote: Compressing objects: 100% (11381/11381), done.
remote: Total 860036 (delta 46251), reused 58081 (delta 46250), pack-reused 801950
Receiving objects: 100% (860036/860036), 205.55 MiB | 233.00 KiB/s, done.
Resolving deltas: 100% (706509/706509), done.
Updating files: 100% (17968/17968), done.

3O5019592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/software/bootloader
$ cd u-boot-socfpga

3O5019592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/software/bootloader/u-boot-socfpga (socfpga_v2022.01)
$ git checkout -b test -t origin/socfpga_v2020.04
Updating files: 100% (13189/13189), done.
Switched to a new branch 'test'
branch 'test' set up to track 'origin/socfpga_v2020.04'.

3O5019592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/software/bootloader/u-boot-socfpga (test)
$ ./arch/arm/mach-socfpga/qts-filter-a10.sh \
> ../../../hps_isw_handoff/hps.xml \
> arch/arm/dts/socfpga_arria10_socdk_sdmmc_handoff.h

3O5019592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/software/bootloader/u-boot-socfpga (test)
$ export CROSS_COMPILE=arm-eabi-

3O5019592@GB1LL2J3E MINGW64 /c/intelFPGA_pro/20.1/embedded/examples/hardware/a10_soc_devkit_ghrd/software/bootloader/u-boot-socfpga (test)
$ make socfpga_arria10_defconfig
makefile:37: *** missing separator.  Stop.
```