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EMIF Maximum Frequency Specification Update

Environment

Quartus Edition
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Quartus® II Subscription Edition
Version Found: 12.1.1
BUILT IN - ARTICLE INTRO SECOND COMPONENT

Critical Issue

Description

This problem affects DDR2 and DDR3 products.

DDR2 and DDR3 interfaces on Arria V GX/GT/SoC or Cyclone V and SoC devices may experience problems achieving timing closure at certain maximum frequencies.

Resolution

The workaround for this issue is to apply the appropriate solution for your configuration, as described below. (The stated performances apply to component topologies only; DDR2 DIMM configurations are not affected, and DDR3 DIMM configurations are not supported.)

DDR2 SDRAM EMIF Maximum Frequency Specification Update for Arria V GX/GT/SoC or Cyclone V and SoC Devices

- **For Arria V GX**, -C5 speed grade device interfacing with a DDR2 SDRAM component with 2 chip selects using hard memory controller at 350 MHz: Upgrade the 400 MHz DDR2 SDRAM component to a 533 MHz DDR2 SDRAM component to achieve an interface frequency of 333 MHz.
- **For Arria V GX**, -C5 speed grade device interfacing with a DDR2 SDRAM component with 1 chip select using hard memory controller at 400 MHz: Upgrade the 400 MHz DDR2 SDRAM component to a 533 MHz DDR2 SDRAM component to achieve the specified maximum frequency. * If you experience timing failure with this configuration in version 13.0 SP1 DP5, file a service request to Altera. This specification is supported in version 13.1.
- **For Arria V GX/GT**, -I5 speed grade device interfacing with a DDR2 SDRAM component with 1 chip select using hard memory controller at 400 MHz: Upgrade the 400 MHz DDR2 SDRAM component to a 533 MHz DDR2 SDRAM component to achieve the specified maximum frequency. * If you experience timing failure with this configuration in version 13.0 SP1 DP5, file a service request to Altera. This specification is supported in version 13.1.

DDR3/DDR3L SDRAM EMIF Maximum Frequency Specification Update for Arria V GX/GT/SoC or Cyclone V and SoC Devices

- **For Cyclone V SoC (SE/SX)**, -A7 speed grade device interfacing with a DDR3 or DDR3L SDRAM component, with 1 chip select using HPS hard memory controller at 400 MHz: Upgrade the 533 MHz DDR3 SDRAM component to a 667 MHz DDR3 SDRAM component to achieve the specified maximum frequency. * If you experience timing failure with this configuration in version 13.0 SP1 DP5, file a service request to Altera. This specification is supported in version 13.1.
- **For Cyclone V GX/E**, -C6 speed grade device interfacing with a DDR3 or DDR3L SDRAM component, with 2 chip selects using hard memory controller at 400 MHz: Upgrade the 533 MHz DDR3 SDRAM component to a 667 MHz DDR3 SDRAM component to achieve the specified maximum frequency.
- **For Cyclone V SoC (SE/SX/ST),** -I7 speed grade device interfacing with a DDR3 or DDR3L SDRAM component, with 1 chip select using HPS hard memory controller at 400 MHz: Upgrade the 533 MHz DDR3 SDRAM component to a 667 MHz DDR3 SDRAM component to achieve the specified maximum frequency.
- **For Arria V GX/GT**, -I3 speed grade device interfacing with a DDR3 or DDR3L SDRAM component, with 1 chip select using hard memory controller at 533 MHz: Upgrade the 533 MHz DDR3 SDRAM component to a 667 MHz DDR3 SDRAM component to achieve the specified maximum frequency.
- **For Arria V GX**, -C4 speed grade device interfacing with a DDR3 or DDR3L SDRAM component, with 1 chip select using hard memory controller at 533 MHz: Upgrade the 533 MHz DDR3 SDRAM component to a 667 MHz DDR3 SDRAM component to achieve the specified maximum frequency.

- **For Arria V GX**, C5 speed grade device interfacing with a DDR3 or DDR3L SDRAM component, with 1 chip select using either soft or hard memory controllers at 533 MHz: Upgrade the 533 MHz DDR3 SDRAM component to a 667 MHz DDR3 SDRAM component to achieve the specified maximum frequency and avoid running memory interface at 425-449 MHz.
- **For Arria V GX**/GT, I5 speed grade device interfacing with a DDR3 or DDR3L SDRAM component, with 1 chip select using either soft or hard memory controllers at 533 MHz: Upgrade the 533 MHz DDR3 SDRAM component to a 667 MHz DDR3 SDRAM component to achieve the specified maximum frequency and avoid running memory interface at 420-449 MHz.

This issue will not be fixed.

The solutions for maximum frequency specifications have been updated in the External Memory Interface Spec Estimator.

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