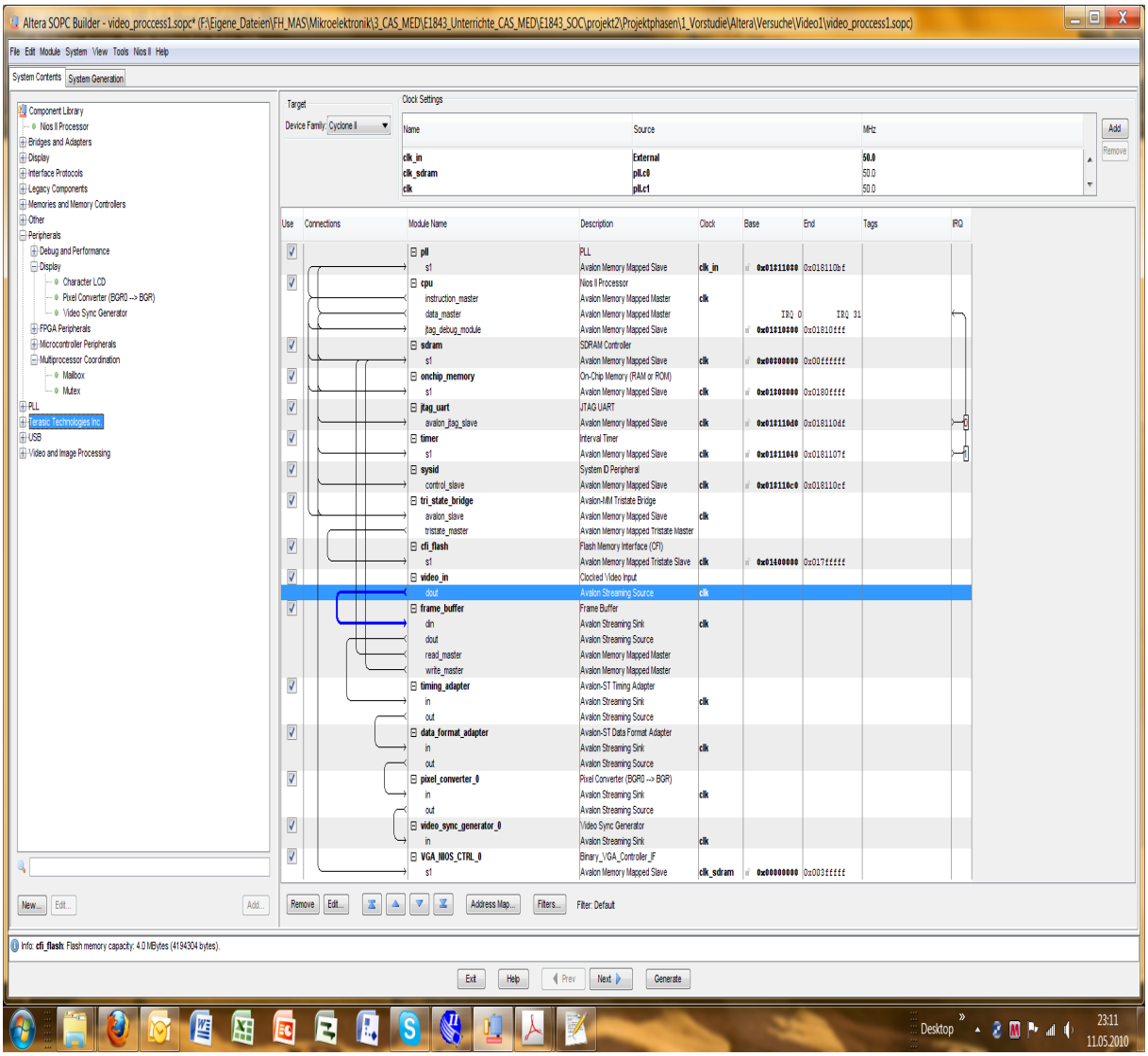
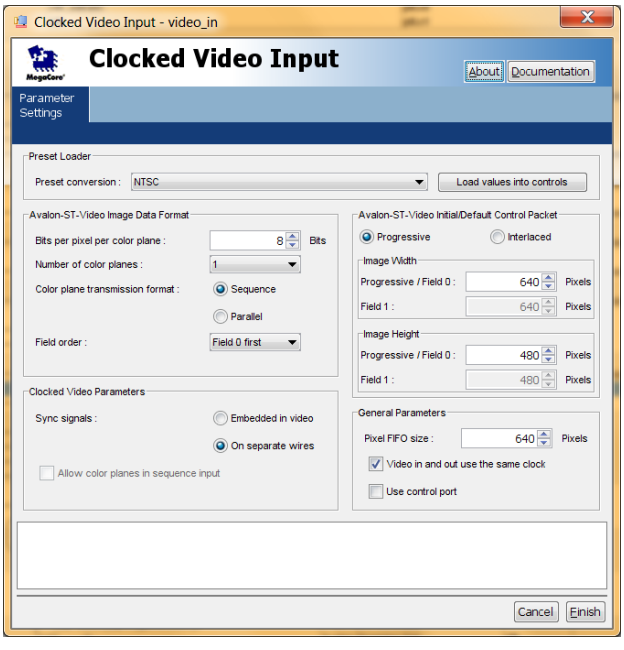
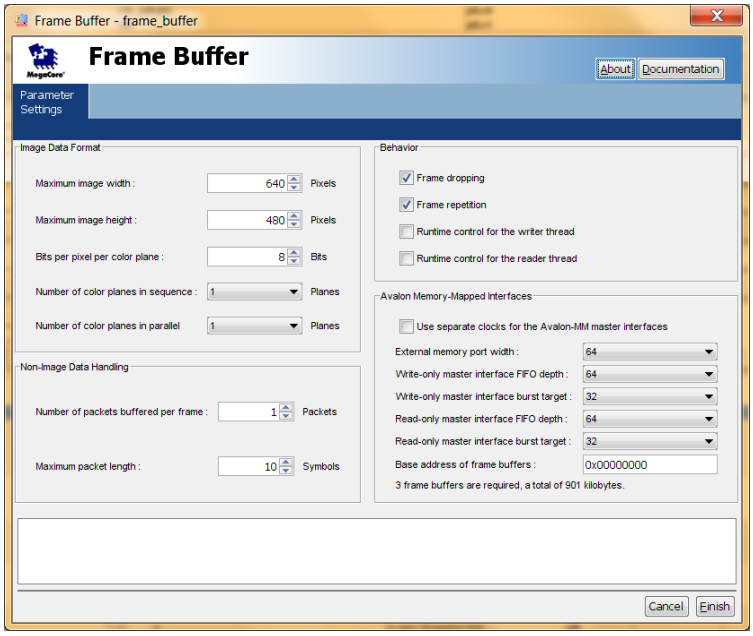
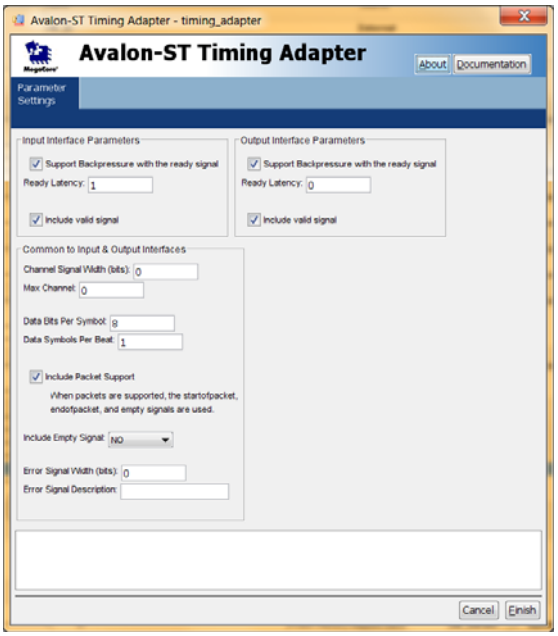
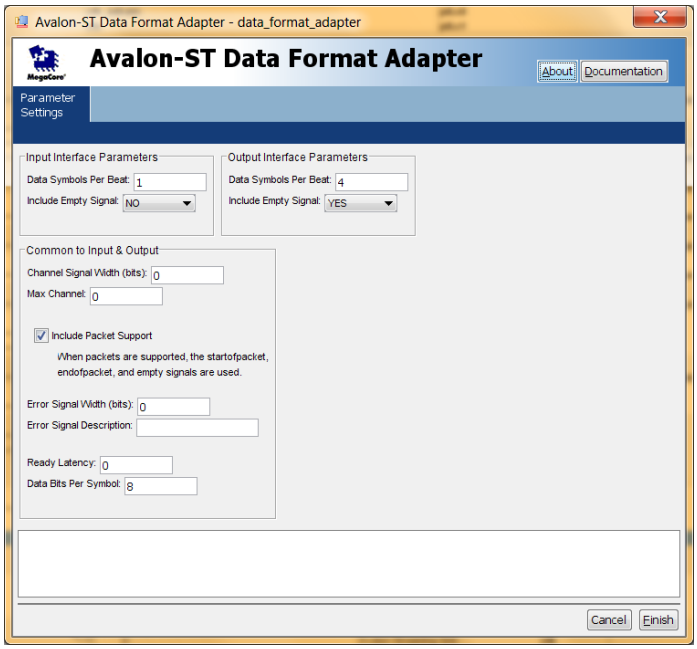
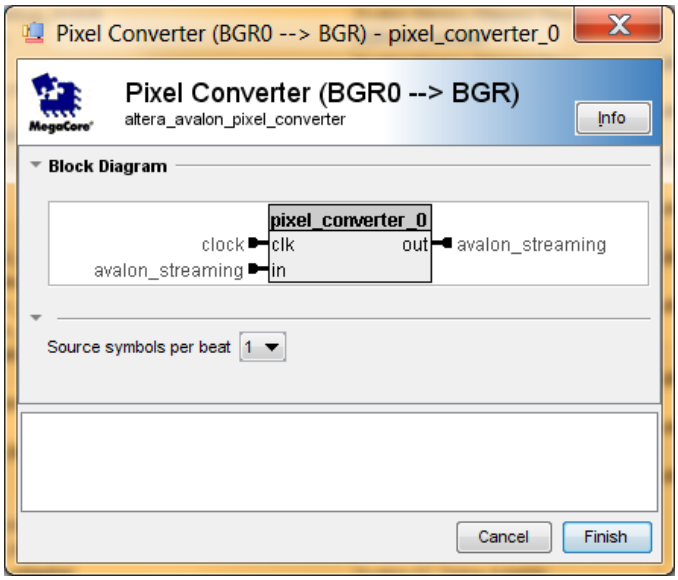

Altera SOPC Builder - video_proccess1.sopc* (F:\Eigene_Dateien\FH_MAS\Mikroelektronik\3_CAS_MED\E1843_Unterrichte_CAS_MED\E1843_SOC\projekt2\Projektphasen\1_Vorstudie\Altera\Versuche\Video1\video_proccess1.sopc)
File Edit Module System View Tools Nios II Help
System Contents
System Generation
Component Library
Nios II Processor
Bridges and Adapters
Display
Interface Protocols
Legacy Components
Memories and Memory Controllers
Other
Peripherals
Debug and Performance
Display
Character LCD
Pixel Converter (BGR0 --> BGR)
Video Sync Generator
FPGA Peripherals
Microcontroller Peripherals
Multiprocessor Coordination
Mailbox
Mutex
PLL
Terasic Technologies Inc.
USB
Video and Image Processing
Target
Device Family: Cyclone II
Clock Settings
Name
Source
MHz
clk_in
External
50.0
clk_sdram
pll.c0
50.0
clk
pll.c1
50.0
Add
Remove
Use
Connections
Module Name
Description
Clock
Base
End
Tags
IRQ
pll
PLL
s1
Avalon Memory Mapped Slave
clk_in
0x01811020
0x018110bf
cpu
Nios II Processor
instruction_master
Avalon Memory Mapped Master
clk
data_master
jtag_debug_module
Avalon Memory Mapped Slave
0x01810800
0x01810fff
sdram
SDRAM Controller
0x00800000
0x00ffffff
onchip_memory
On-Chip Memory (RAM or ROM)
0x01800000
0x01801fff
jtag_uart
JTAG UART
avalon_jtag_slave
0x018110d0
0x018110df
timer
Interval Timer
0x01811040
0x0181107f
sysid
System ID Peripheral
control_slave
0x018110c0
0x018110cf
tri_state_bridge
Avalon-MM Tristate Bridge
avalon_slave
tristate_master
Avalon Memory Mapped Tristate Master
cfi_flash
Flash Memory Interface (CFI)
0x01400000
0x017fffff
video_in
Clocked Video Input
dout
Avalon Streaming Source
frame_buffer
Frame Buffer
din
Avalon Streaming Sink
read_master
write_master
timing_adapter
Avalon-ST Timing Adapter
in
out
data_format_adapter
Avalon-ST Data Format Adapter
pixel_converter_0
Pixel Converter (BGR0 --> BGR)
video_sync_generator_0
Video Sync Generator
VGA_HOS_CTRL_0
Binary_VGA_Controller_IF
clk_sdram
0x00800000
0x00bfffff
New...
Edit...
Add...
Remove
Edit...
Address Map...
Filters...
Filter: Default
Info: cfi_flash: Flash memory capacity: 4.0 MBytes (4194304 bytes).
Exit
Help
Prev
Next
Generate
Desktop
23:11
11.05.2010

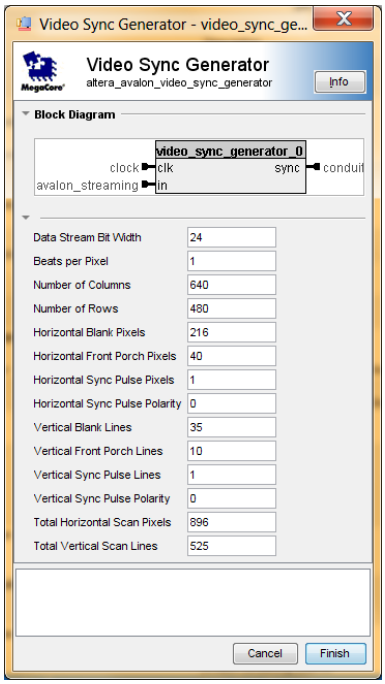

Clocked Video Input - video_in
Clocked Video Input
About
Documentation
Parameter Settings
Preset Loader
Preset conversion :
NTSC
Load values into controls
Avalon-ST-Video Image Data Format
Bits per pixel per color plane :
8
Bits
Number of color planes :
1
Color plane transmission format :
Sequence
Parallel
Field order :
Field 0 first
Avalon-ST-Video Initial/Default Control Packet
Progressive
Interlaced
Image Width
Progressive / Field 0 :
640
Pixels
Field 1 :
640
Pixels
Image Height
Progressive / Field 0 :
480
Pixels
Field 1 :
480
Pixels
Clocked Video Parameters
Sync signals :
Embedded in video
On separate wires
Allow color planes in sequence input
General Parameters
Pixel FIFO size :
640
Pixels
Video in and out use the same clock
Use control port
Cancel
Finish

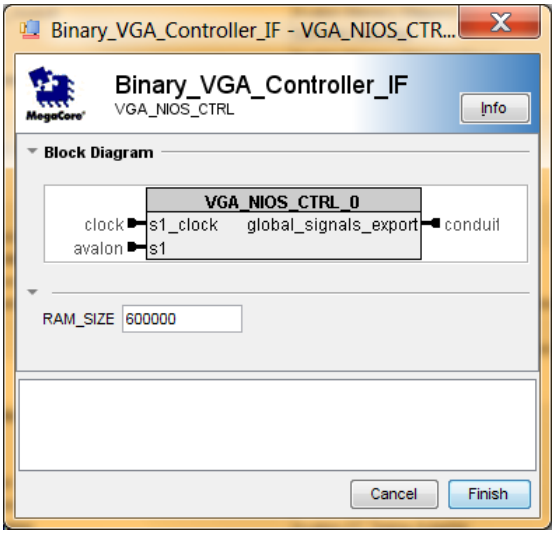

Frame Buffer - frame_buffer
Frame Buffer
About
Documentation
Parameter Settings
Image Data Format
Maximum image width : 640 Pixels
Maximum image height : 480 Pixels
Bits per pixel per color plane : 8 Bits
Number of color planes in sequence : 1 Planes
Number of color planes in parallel : 1 Planes
Non-Image Data Handling
Number of packets buffered per frame : 1 Packets
Maximum packet length : 10 Symbols
Behavior
Frame dropping
Frame repetition
Runtime control for the writer thread
Runtime control for the reader thread
Avalon Memory-Mapped Interfaces
Use separate clocks for the Avalon-MM master interfaces
External memory port width : 64
Write-only master interface FIFO depth : 64
Write-only master interface burst target : 32
Read-only master interface FIFO depth : 64
Read-only master interface burst target : 32
Base address of frame buffers : 0x00000000
3 frame buffers are required, a total of 901 kilobytes.
Cancel
Finish

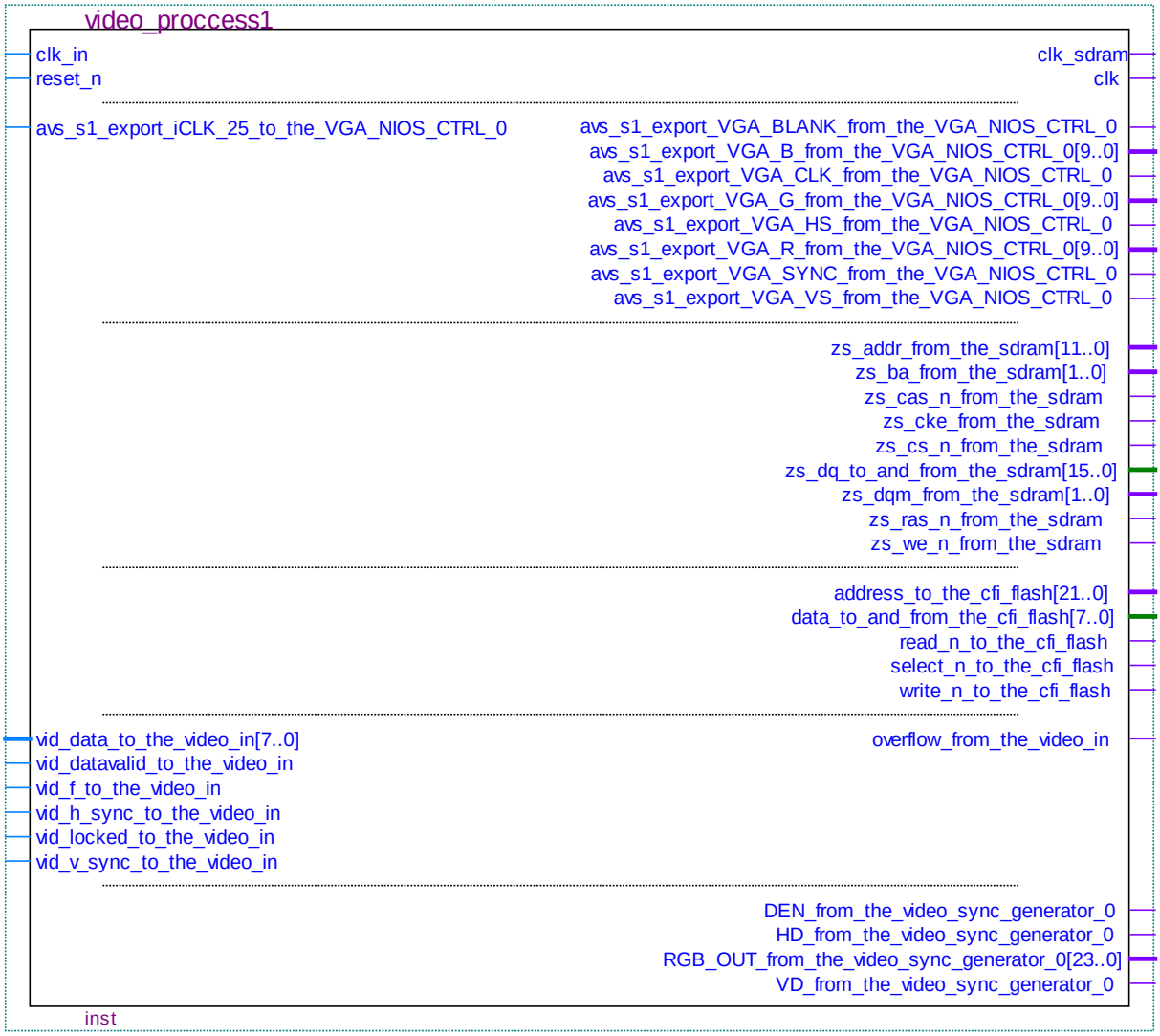

Avalon-ST Timing Adapter - timing_adapter
Avalon-ST Timing Adapter
About
Documentation
Parameter Settings
Input Interface Parameters
Support Backpressure with the ready signal
Ready Latency: 1
Include valid signal
Output Interface Parameters
Support Backpressure with the ready signal
Ready Latency: 0
Include valid signal
Common to Input & Output Interfaces
Channel Signal Width (bits): 0
Max Channel: 0
Data Bits Per Symbol: 8
Data Symbols Per Beat: 1
Include Packet Support
When packets are supported, the startofpacket, endofpacket, and empty signals are used.
Include Empty Signal: NO
Error Signal Width (bits): 0
Error Signal Description:
Cancel
Finish


Avalon-ST Data Format Adapter - data_format_adapter
Avalon-ST Data Format Adapter
About
Documentation
Parameter Settings
Input Interface Parameters
Data Symbols Per Beat: 1
Include Empty Signal: NO
Output Interface Parameters
Data Symbols Per Beat: 4
Include Empty Signal: YES
Common to Input & Output
Channel Signal Width (bits): 0
Max Channel: 0
Include Packet Support
When packets are supported, the startofpacket, endofpacket, and empty signals are used.
Error Signal Width (bits): 0
Error Signal Description:
Ready Latency: 0
Data Bits Per Symbol: 8
Cancel
Finish


Pixel Converter (BGR0 --> BGR) - pixel_converter_0
Pixel Converter (BGR0 --> BGR)
altera_avalon_pixel_converter
Info
Block Diagram
pixel_converter_0
clock
clk
out
avalon_streaming
avalon_streaming
in
Source symbols per beat 1
Cancel
Finish


Video Sync Generator - video_sync_ge...
Video Sync Generator
altera_avalon_video_sync_generator
Info
Block Diagram
video_sync_generator_0
clock
clk
sync
conduit
avalon_streaming
in
Data Stream Bit Width 24
Beats per Pixel 1
Number of Columns 640
Number of Rows 480
Horizontal Blank Pixels 216
Horizontal Front Porch Pixels 40
Horizontal Sync Pulse Pixels 1
Horizontal Sync Pulse Polarity 0
Vertical Blank Lines 35
Vertical Front Porch Lines 10
Vertical Sync Pulse Lines 1
Vertical Sync Pulse Polarity 0
Total Horizontal Scan Pixels 896
Total Vertical Scan Lines 525
Cancel
Finish


Binary_VGA_Controller_IF - VGA_NIOS_CTR...
Binary_VGA_Controller_IF
VGA_NIOS_CTRL
Info
Block Diagram
VGA_NIOS_CTRL_0
clock
s1_clock
global_signals_export
conduit
avalon
s1
RAM_SIZE 600000
Cancel
Finish


video_proccess1
clk_in
reset_n
avs_s1_export_iCLK_25_to_the_VGA_NIOS_CTRL_0
vid_data_to_the_video_in[7..0]
vid_datavalid_to_the_video_in
vid_f_to_the_video_in
vid_h_sync_to_the_video_in
vid_locked_to_the_video_in
vid_v_sync_to_the_video_in
clk_sdram
clk
avs_s1_export_VGA_BLANK_from_the_VGA_NIOS_CTRL_0
avs_s1_export_VGA_B_from_the_VGA_NIOS_CTRL_0[9..0]
avs_s1_export_VGA_CLK_from_the_VGA_NIOS_CTRL_0
avs_s1_export_VGA_G_from_the_VGA_NIOS_CTRL_0[9..0]
avs_s1_export_VGA_HS_from_the_VGA_NIOS_CTRL_0
avs_s1_export_VGA_R_from_the_VGA_NIOS_CTRL_0[9..0]
avs_s1_export_VGA_SYNC_from_the_VGA_NIOS_CTRL_0
avs_s1_export_VGA_VS_from_the_VGA_NIOS_CTRL_0
zs_addr_from_the_sdram[11..0]
zs_ba_from_the_sdram[1..0]
zs_cas_n_from_the_sdram
zs_cke_from_the_sdram
zs_cs_n_from_the_sdram
zs_dq_to_and_from_the_sdram[15..0]
zs_dqm_from_the_sdram[1..0]
zs_ras_n_from_the_sdram
zs_we_n_from_the_sdram
address_to_the_cfi_flash[21..0]
data_to_and_from_the_cfi_flash[7..0]
read_n_to_the_cfi_flash
select_n_to_the_cfi_flash
write_n_to_the_cfi_flash
overflow_from_the_video_in
DEN_from_the_video_sync_generator_0
HD_from_the_video_sync_generator_0
RGB_OUT_from_the_video_sync_generator_0[23..0]
VD_from_the_video_sync_generator_0
inst