Stratix 10 SoC FPGA Development Kit Board

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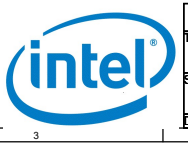
REV	DATE	PAGES	DESCRIPTION
A.0 release			Modified from150-0321319 RevA1.
		50,58,59,60,61,64	Change M12Vto3V3,VCCERAM,VCC_HPS,VCCPT,VCCT, VCCR using Enpirion devices
		35	Swap SDI_SDA,SDI_SCL
		56	Connect S10_VCCFAULT for U55 (pin25,26)
		30	Change FPGA symbol based on new pinout for TSD0 and TSD1
		38	Add new temp sense chip U116 for TSD1
		38	Group EM2130 I2C bus and add dip switch SW8 for isolation
	10/12/17	50,60	Change C1677,C1678, C1771,C1772 to 22uF Cer cap 16V
B.0 release			
		50	Change R5246 to 12K and I2C addres to 4B
		9	Ground MT1 to MT3
		58	Change C1698 Capacitor to diff Agile number
		40	REMOVED Parrallel Flash



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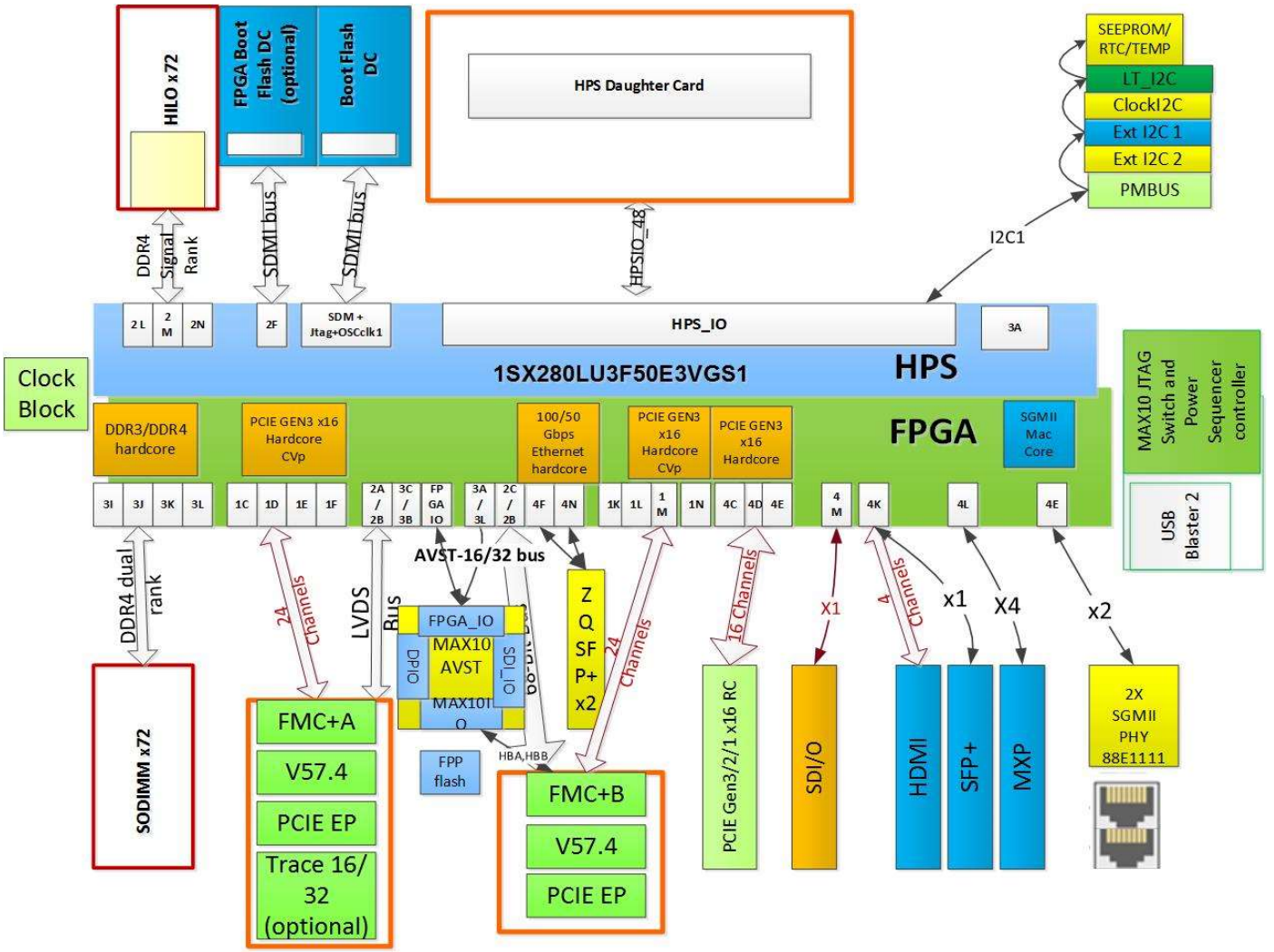
Stratix 10 Dev Kit Block Diagram



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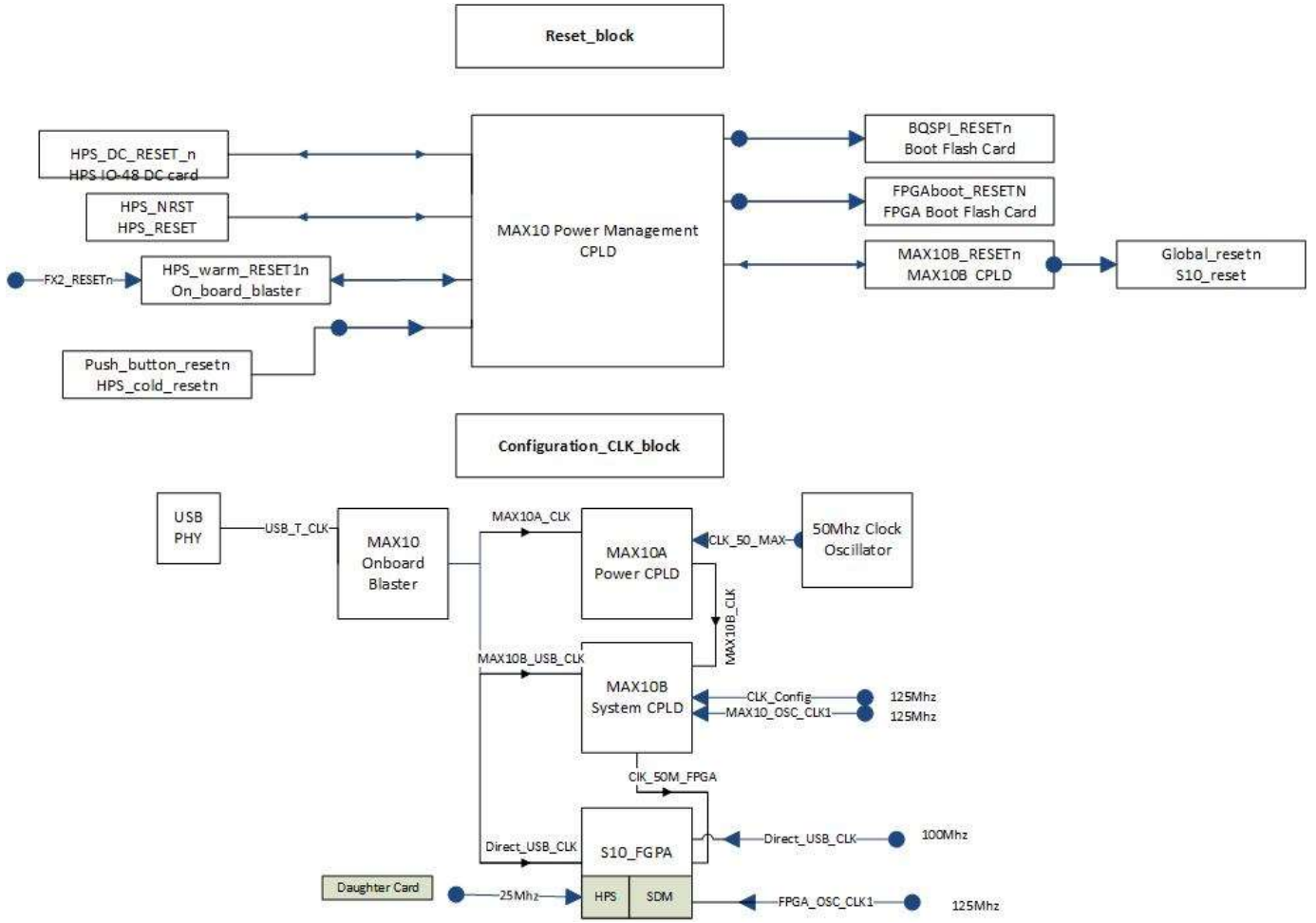
S10soc Dev Kit Reset Block



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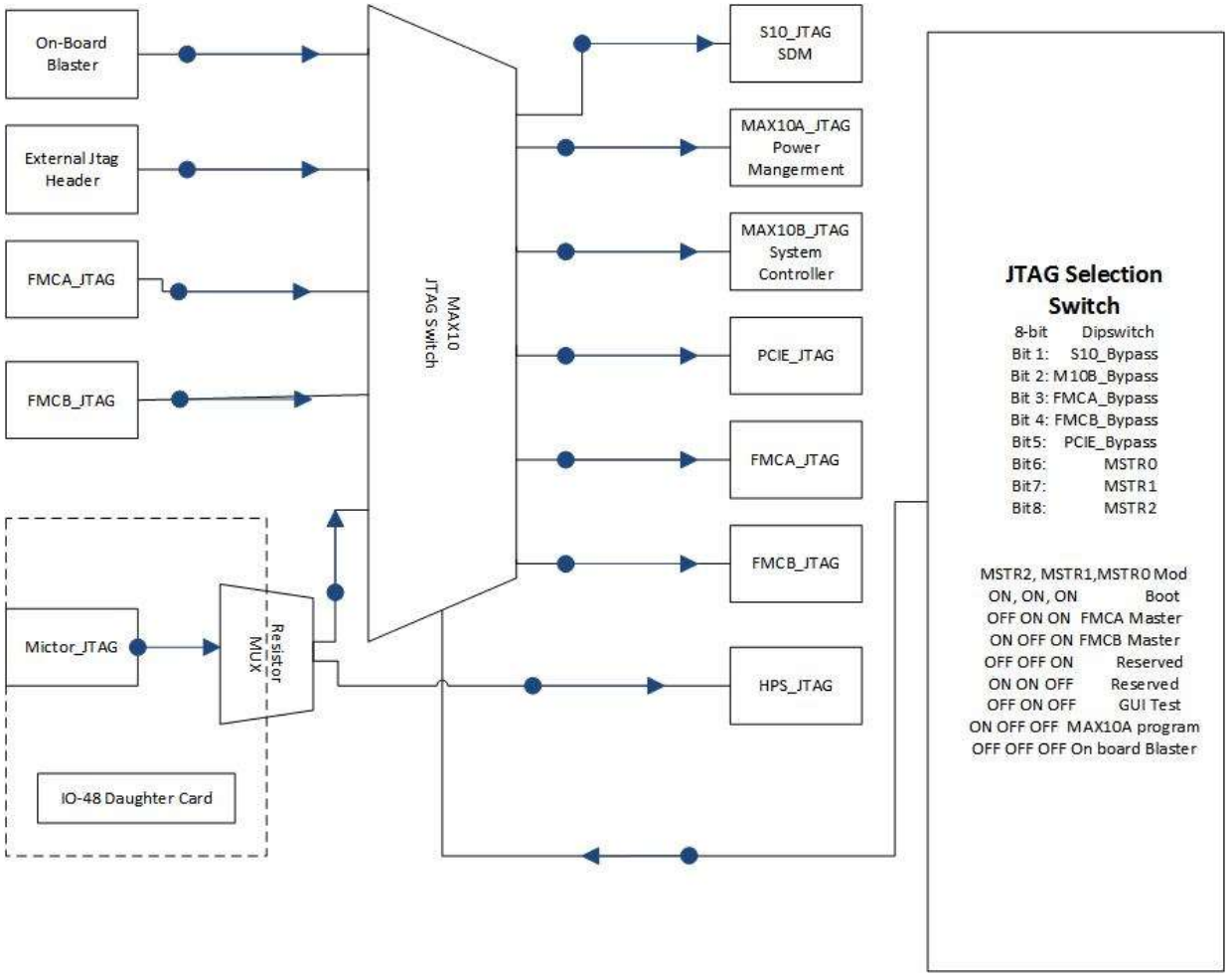
JTAG Connection Diagram



JTAG Selection Switch

8-bit Dipswitch
Bit 1: S10_Bypass
Bit 2: M10B_Bypass
Bit 3: FMCA_Bypass
Bit 4: FMCB_Bypass
Bit5: PCIE_Bypass
Bit6: MSTR0
Bit7: MSTR1
Bit8: MSTR2

MSTR2, MSTR1,MSTR0 Mod
ON, ON, ON Boot
OFF ON ON FMCA Master
ON OFF ON FMCB Master
OFF OFF ON Reserved
ON ON OFF Reserved
OFF ON OFF GUI Test
ON OFF OFF MAX10A program
OFF OFF OFF On board Blaster

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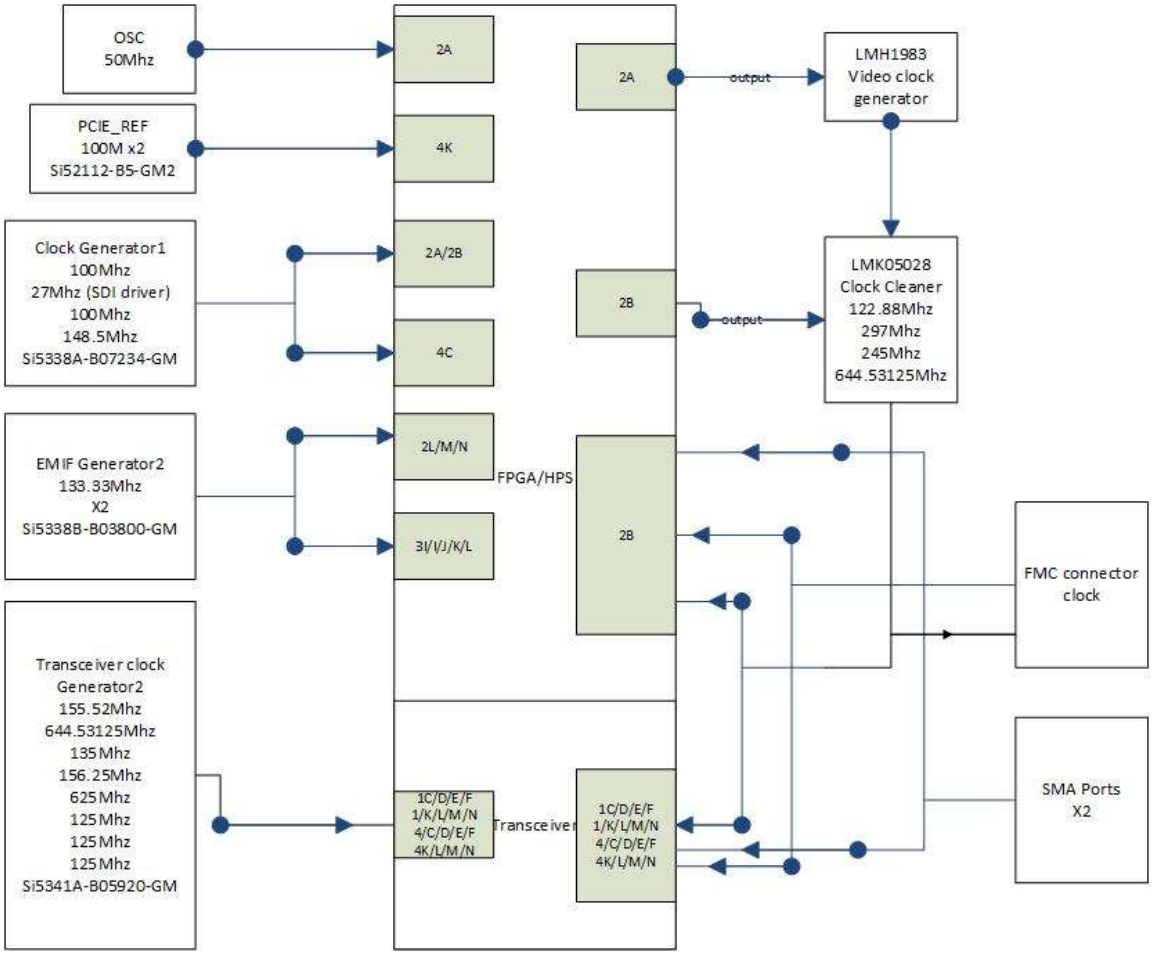
Stratix 10 Dev Kit Clock Connection



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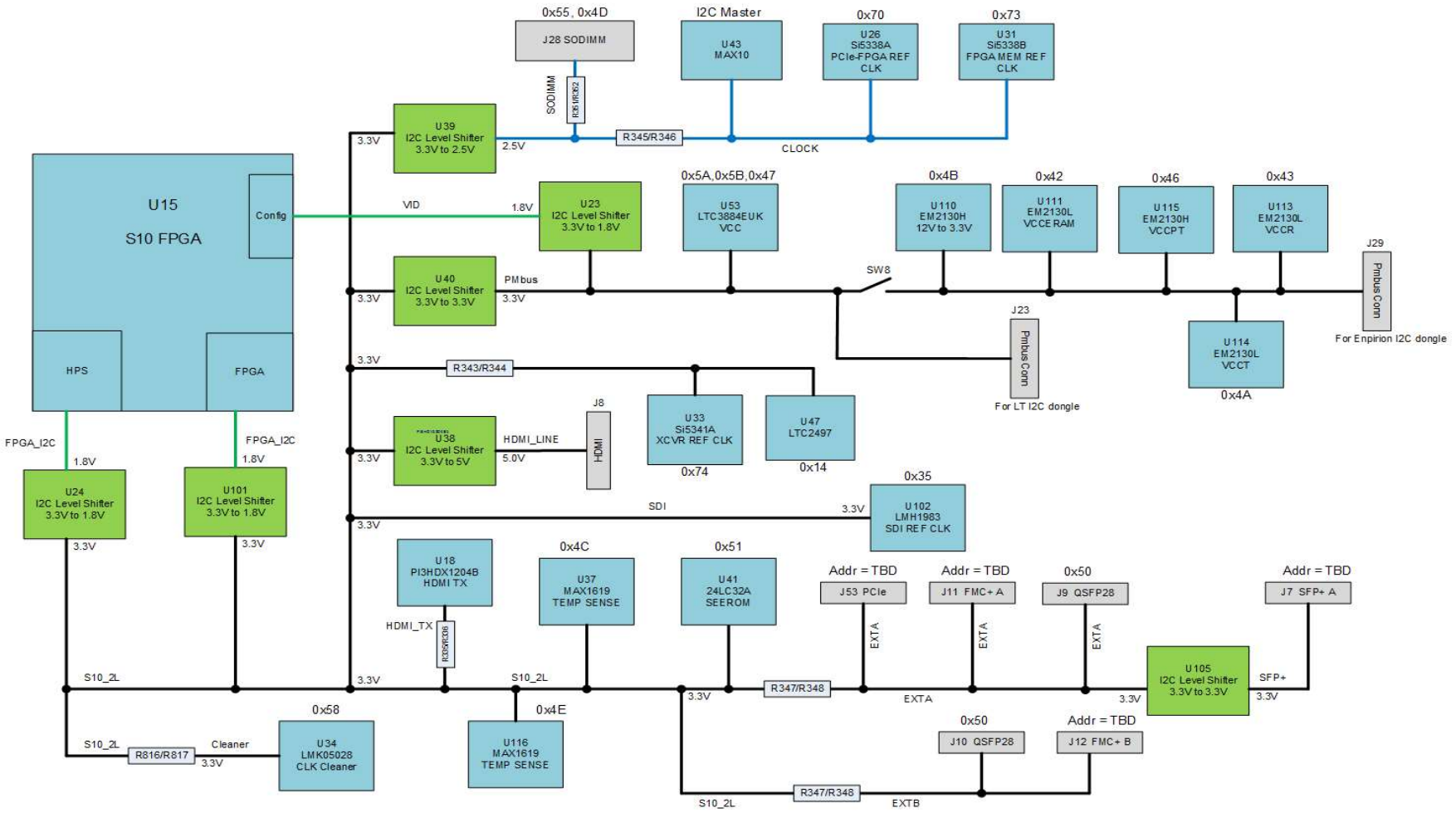
S10 SoC I2C Bus Connection



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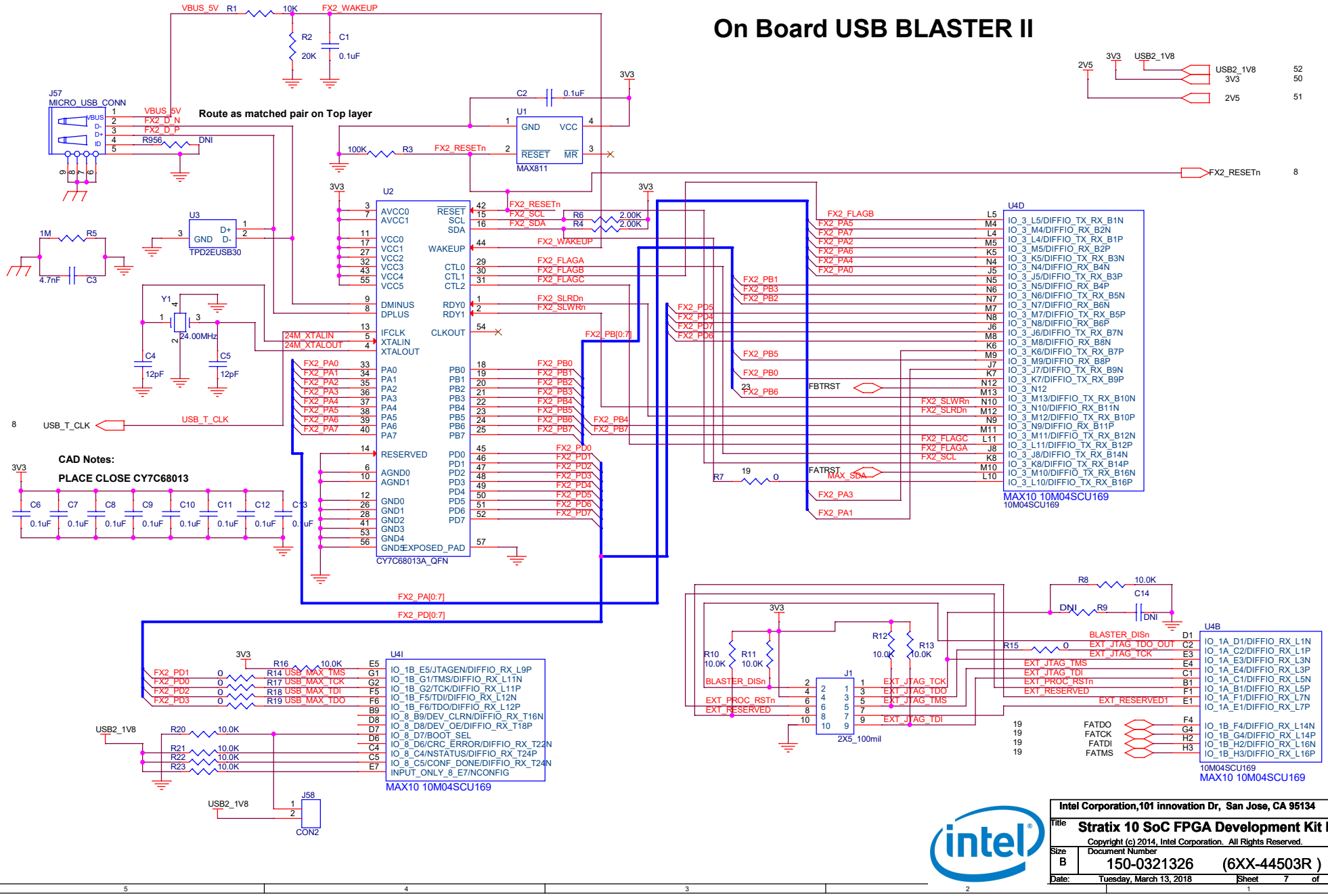
On Board USB BLASTER II



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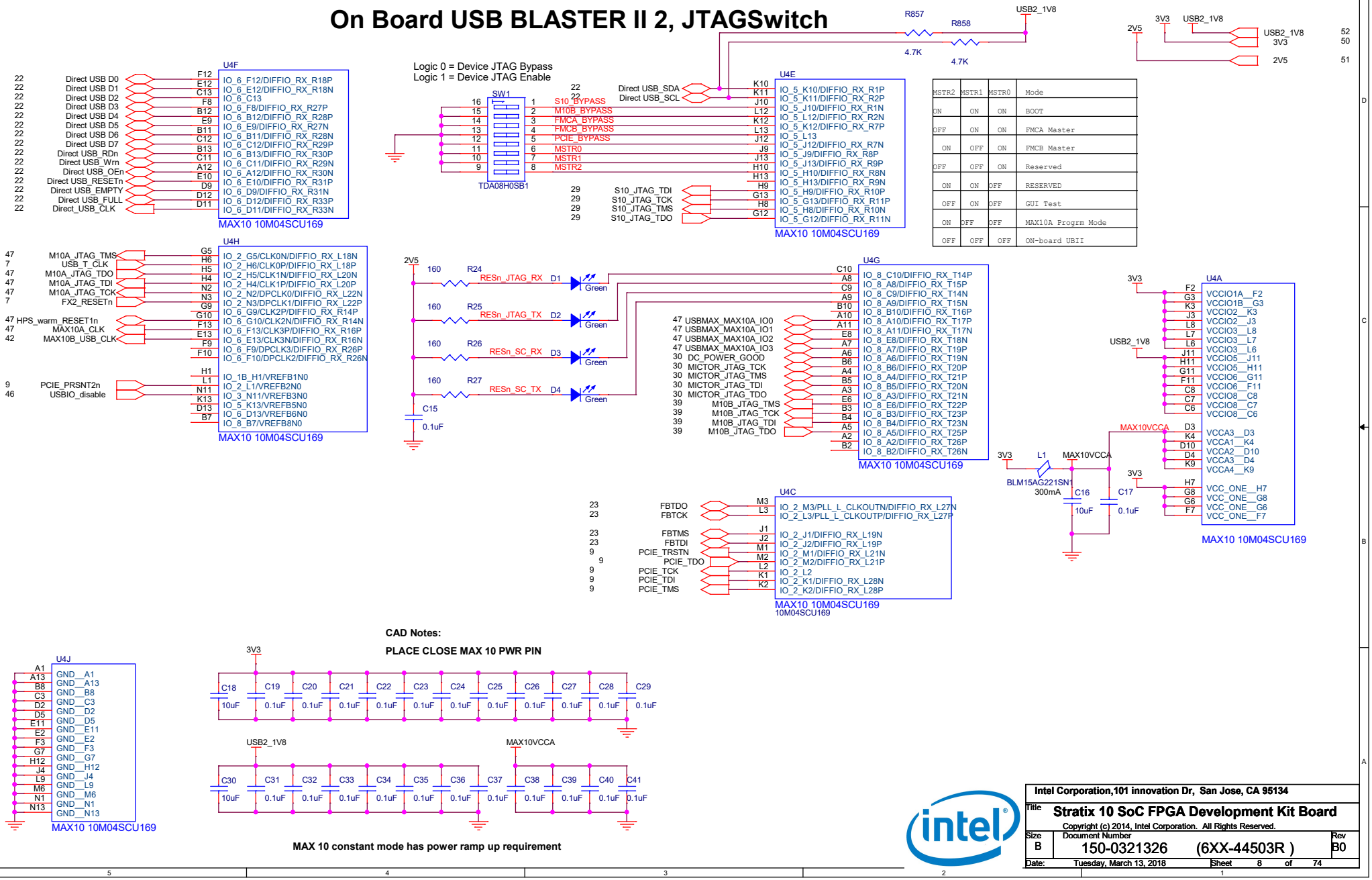
On Board USB BLASTER II 2, JTAGSwitch



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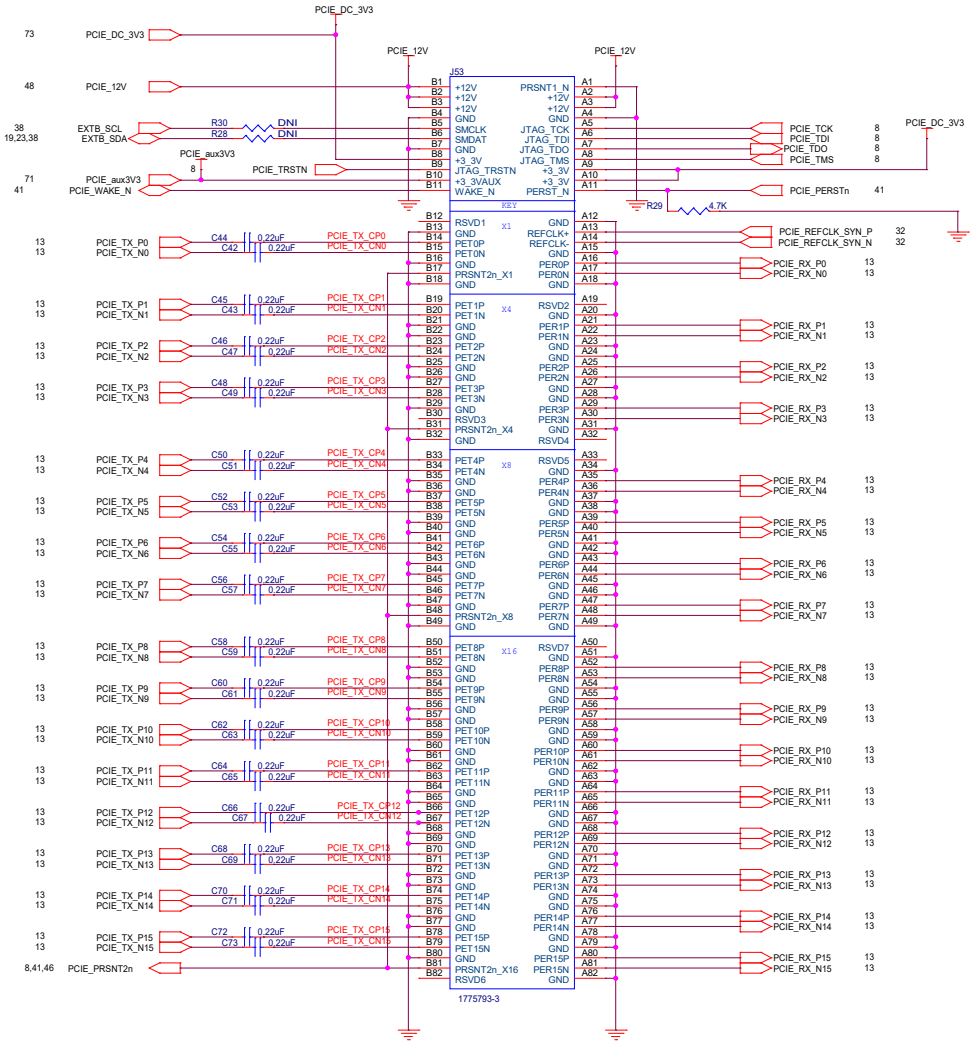
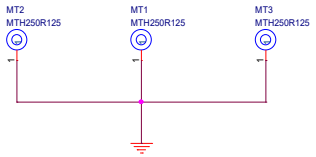
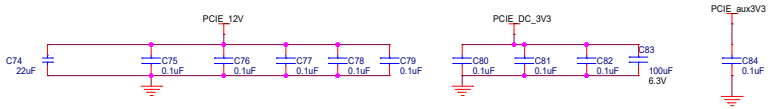
PCI Express GEN3 X 16 Connector





75-ohm to 100-ohm XCVR traces.



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10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber

SGMII Mode (default)

88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement

DVDD = 1.0V
DVDD = 1.2V

ENET_DVDD = 1.0V/0.207A

Place near 88E1111 PHY

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Title: Stratix 10 SoC FPGA Development Kit Board

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10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber

88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement

SGMII Mode (default)

Place near 88E1111 PHY

ENET_DVDD = 1.0V/0.207A

DVDD = 1.0V
DVDD = 1.2V

Ethernet2_CASE_GND

LTC3025-1

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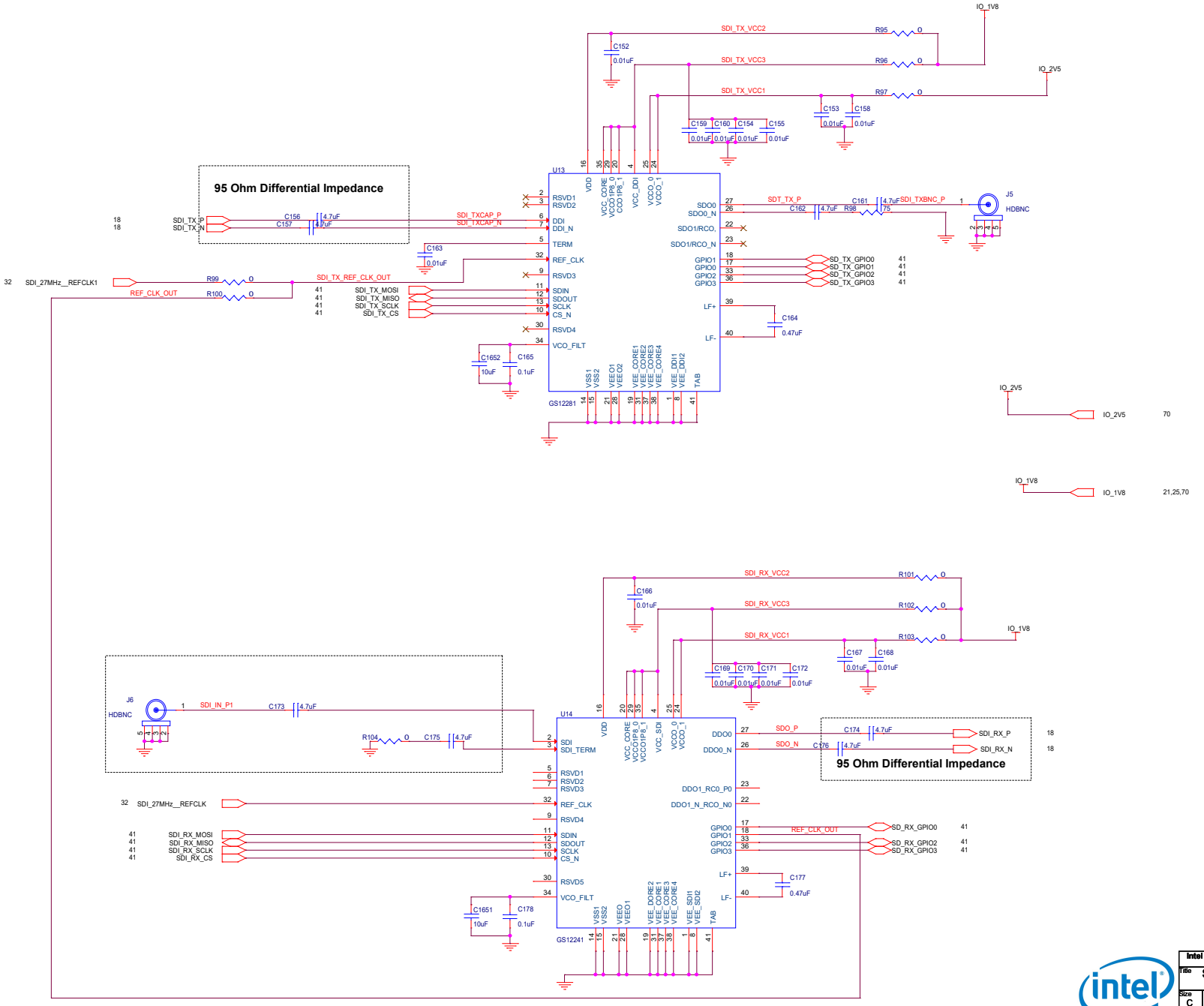
SDI Cable Driver, Equalizer, and SMB



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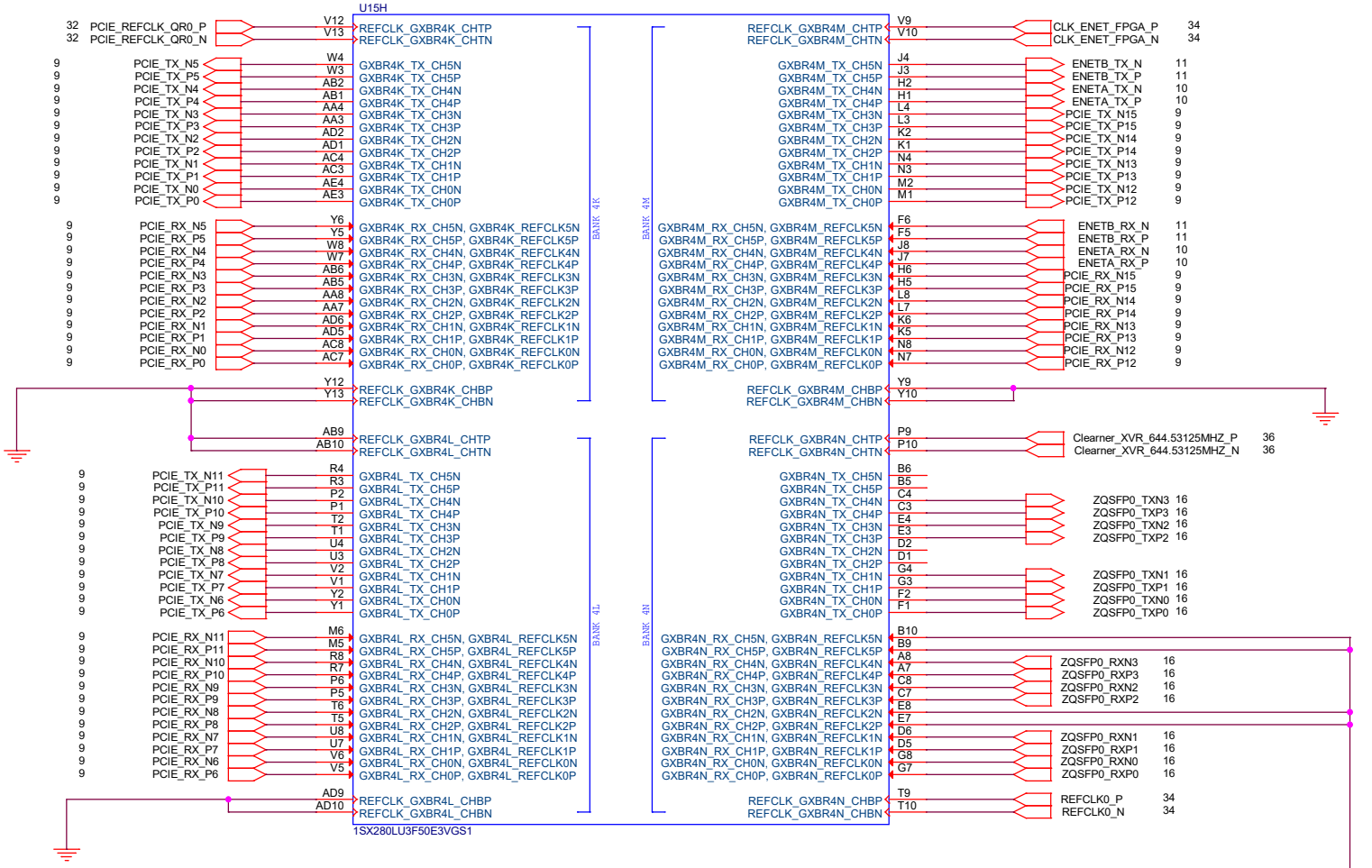
Stratix 10 XCVR Banks - 4K/L/M/N



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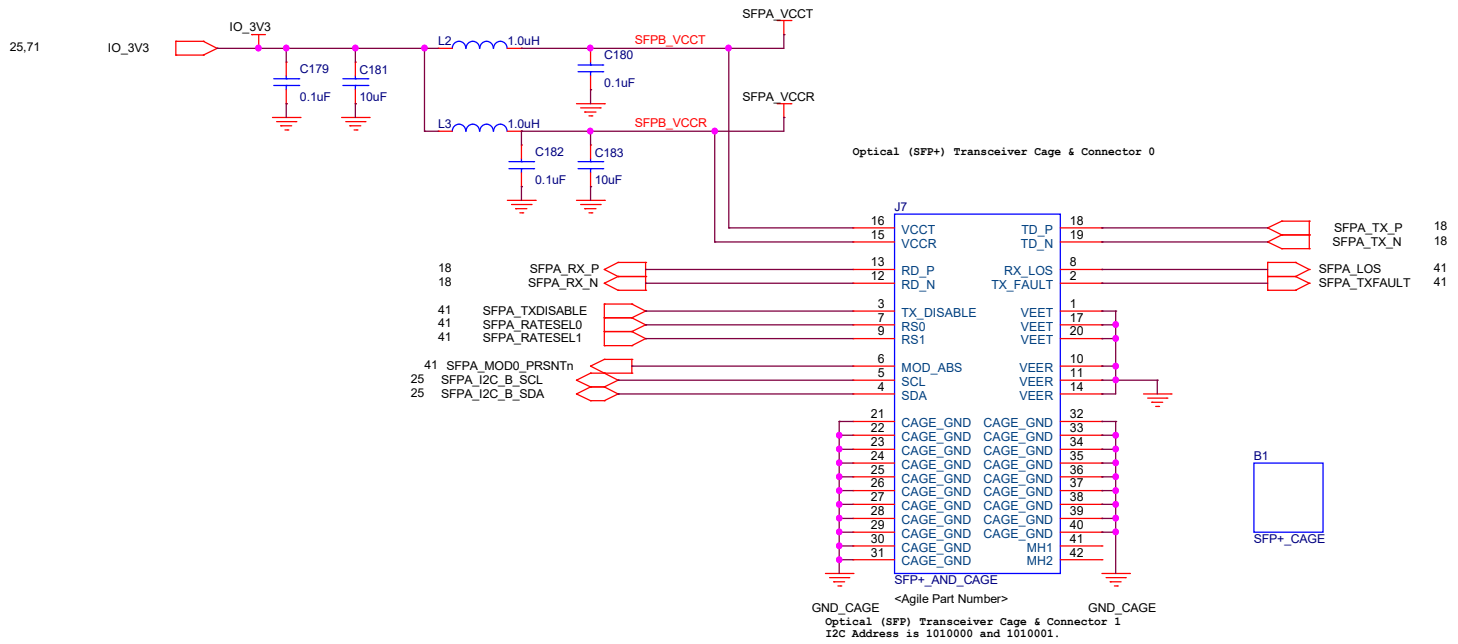
Small Form Factor Pluggable Plus (SFP+) Port A



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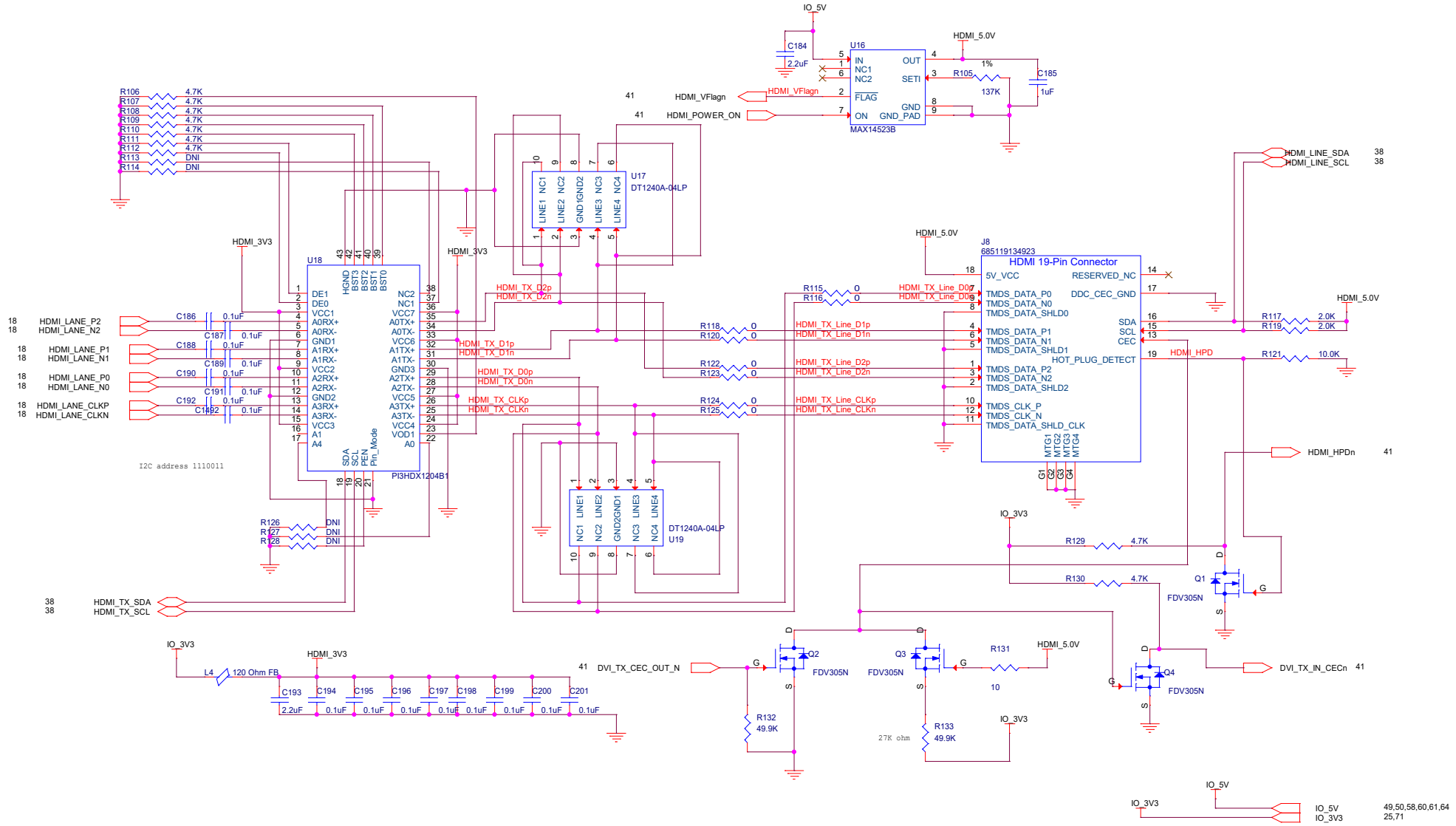
HDMI (VIDEO ONLY)



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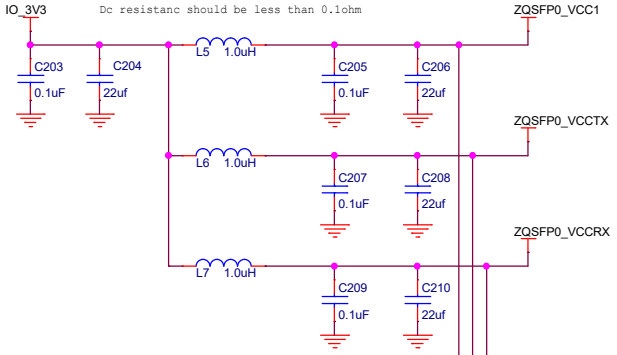
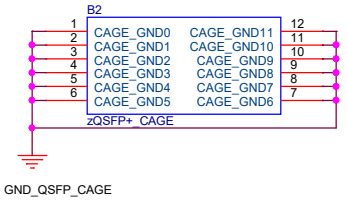
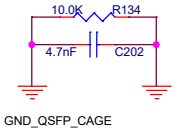
QSFP28 Interface 0 & MXP Cable connection

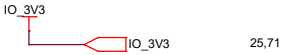


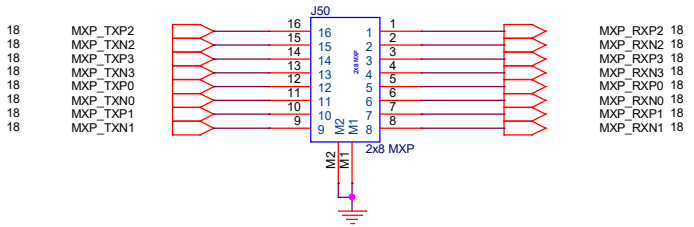
P and N can be swapped for better SI performance

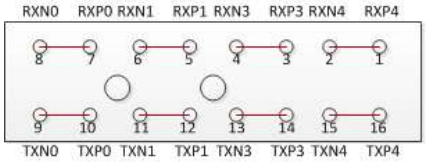




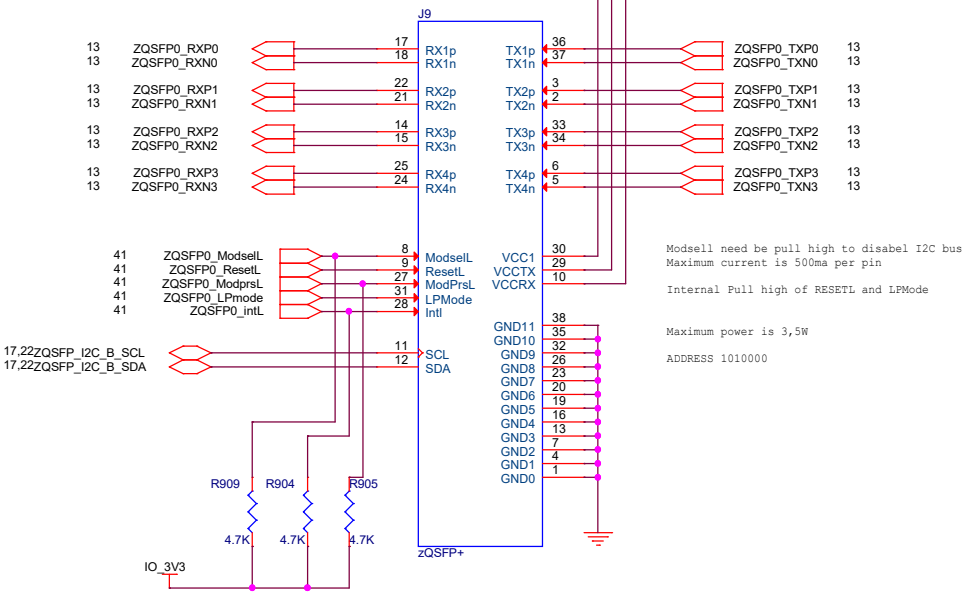
Cage GND on top layer







QSFP28 Interface



Modsell need be pull high to disabel I2C bus
Maximum current is 500ma per pin

Internal Pull high of RESETL and LPMode

Maximum power is 3,5W

ADDRESS 1010000

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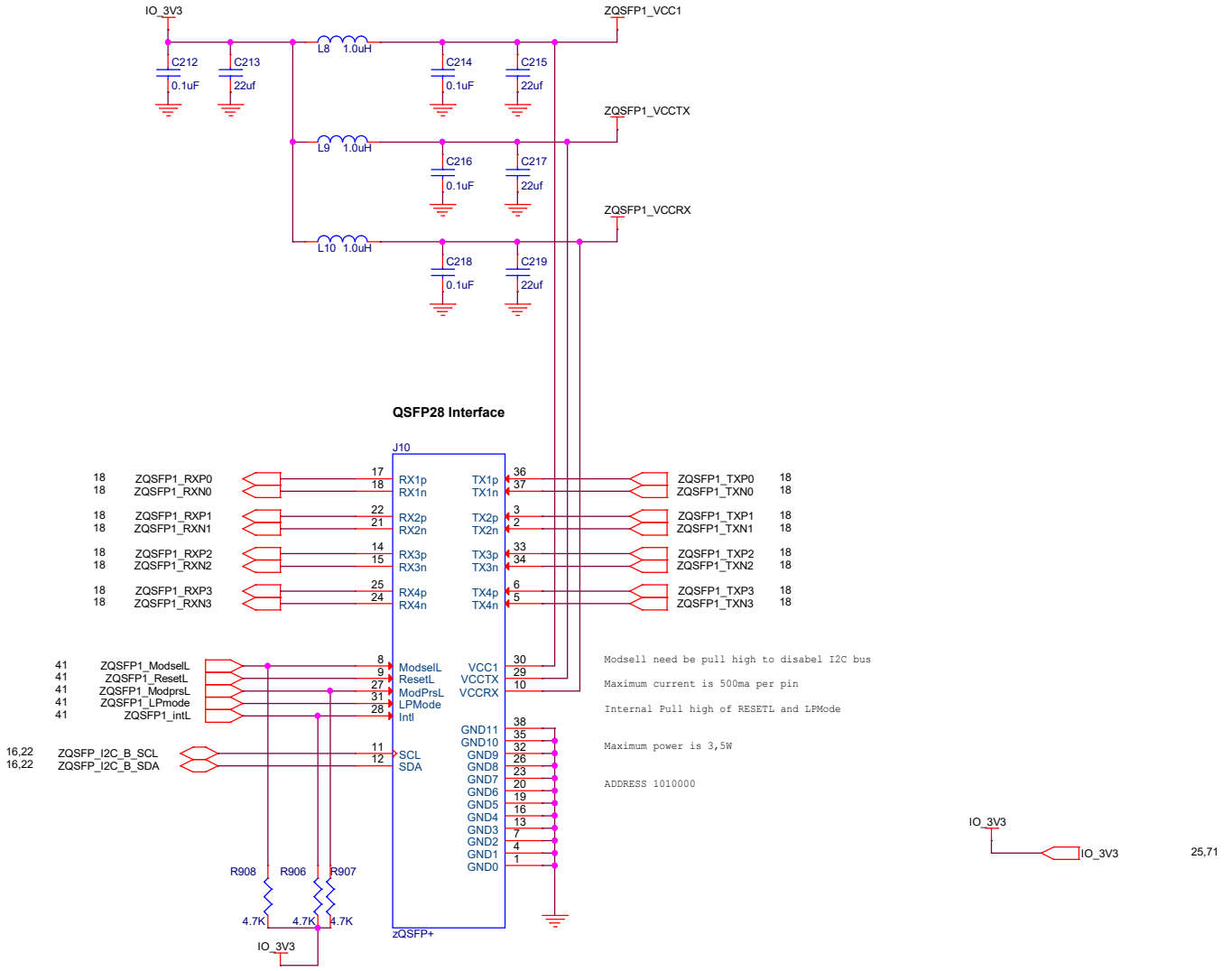
QSFP28 Interface 1

Dc resistanc should be less than 0.1ohm



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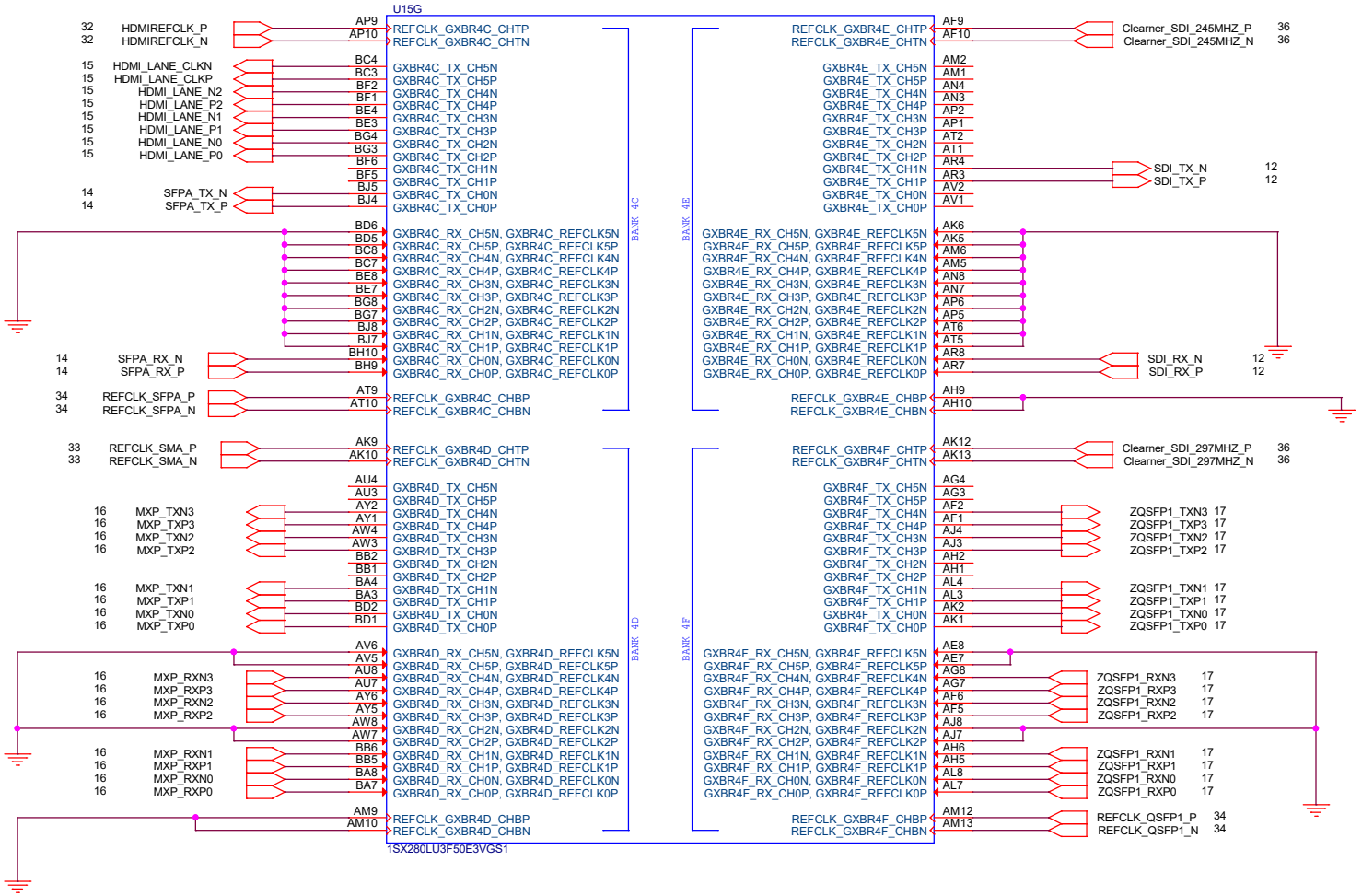
S10 XCVR Banks - 4C/D/E/F



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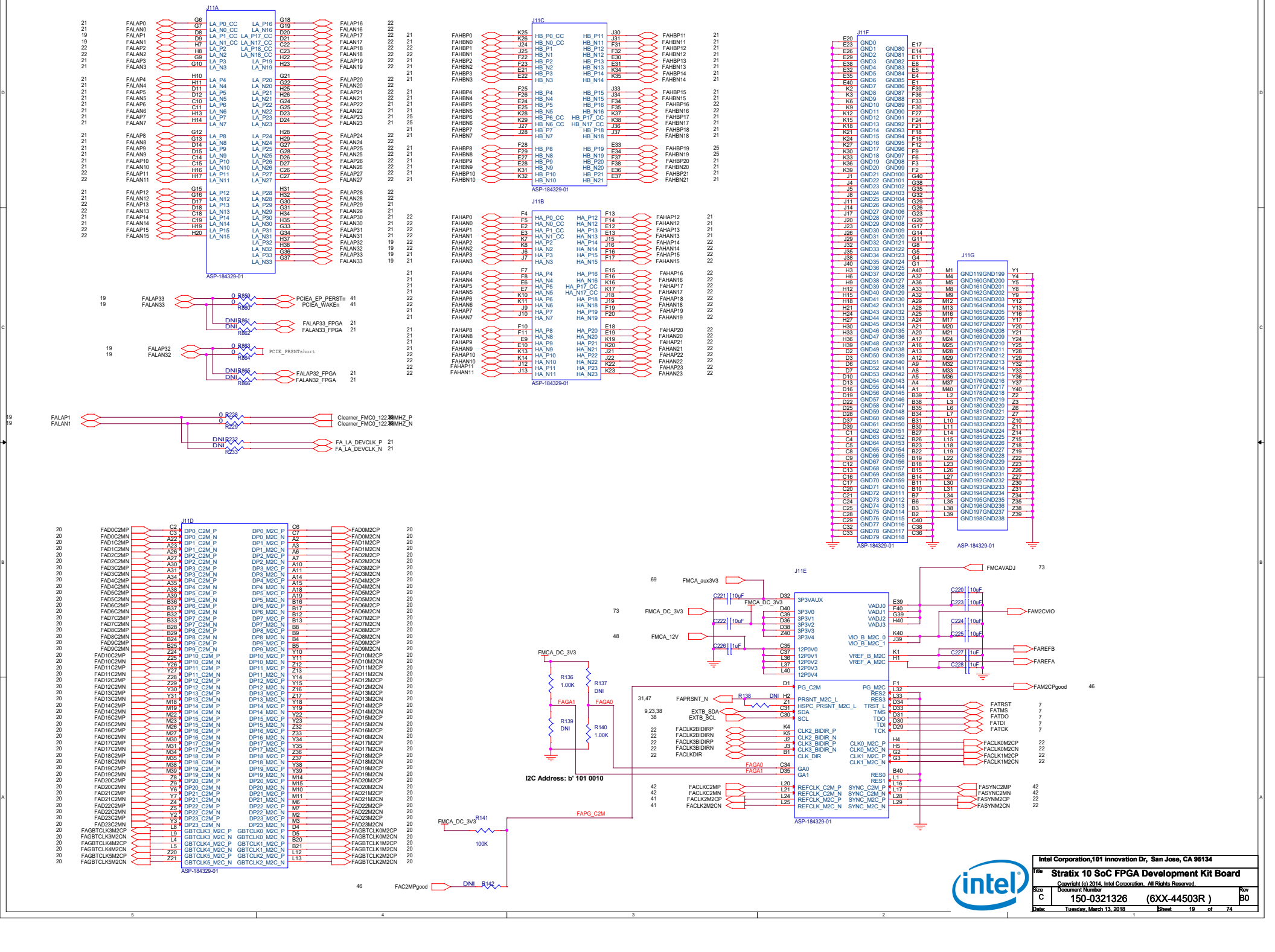
FMC Port A


J11A
J11C
J11B
J11F
J11G
J11D
J11E
ASP-184329-01
I2C Address: b' 101 0010
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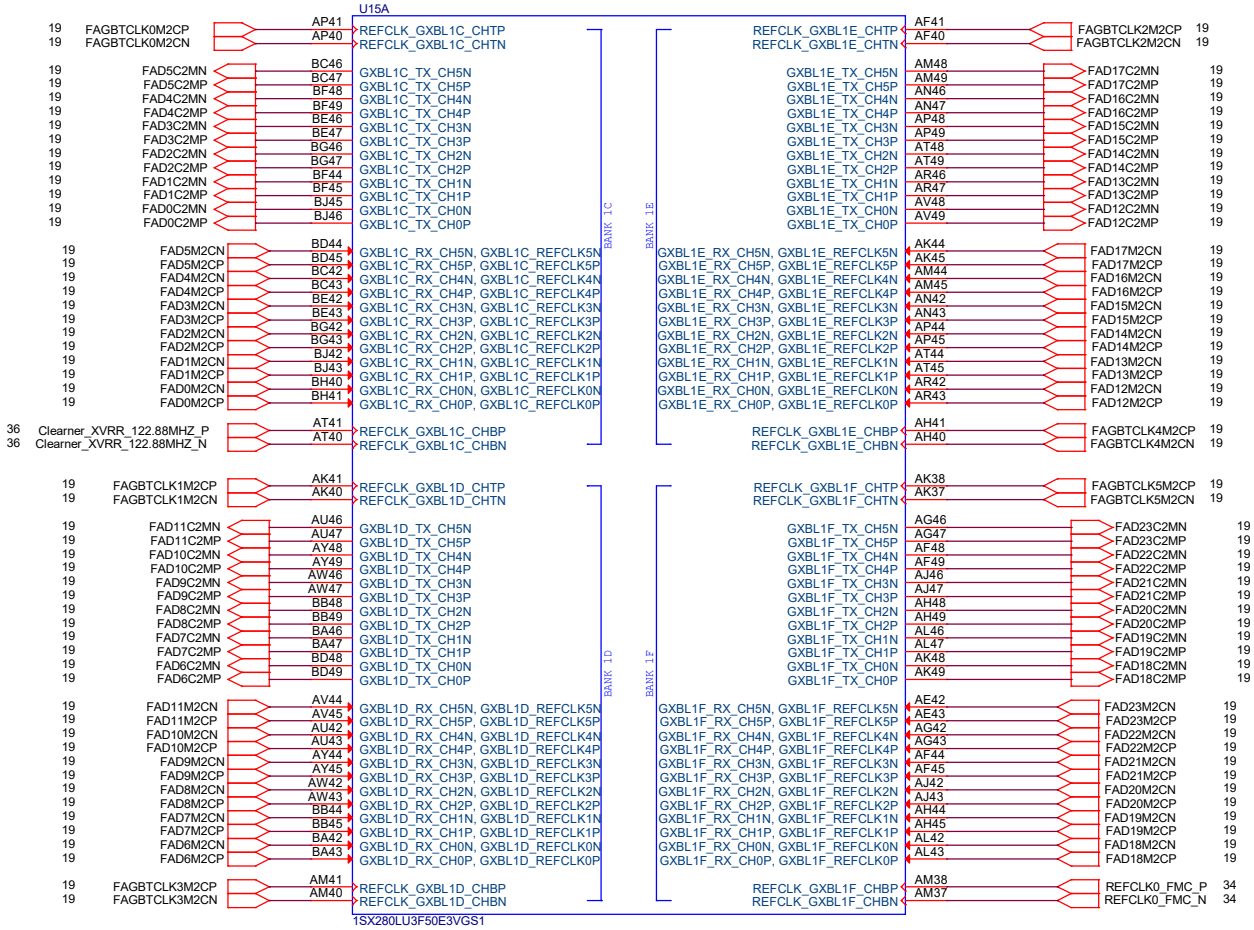
Stratix 10 XCVR Banks - 1C/D/E/F



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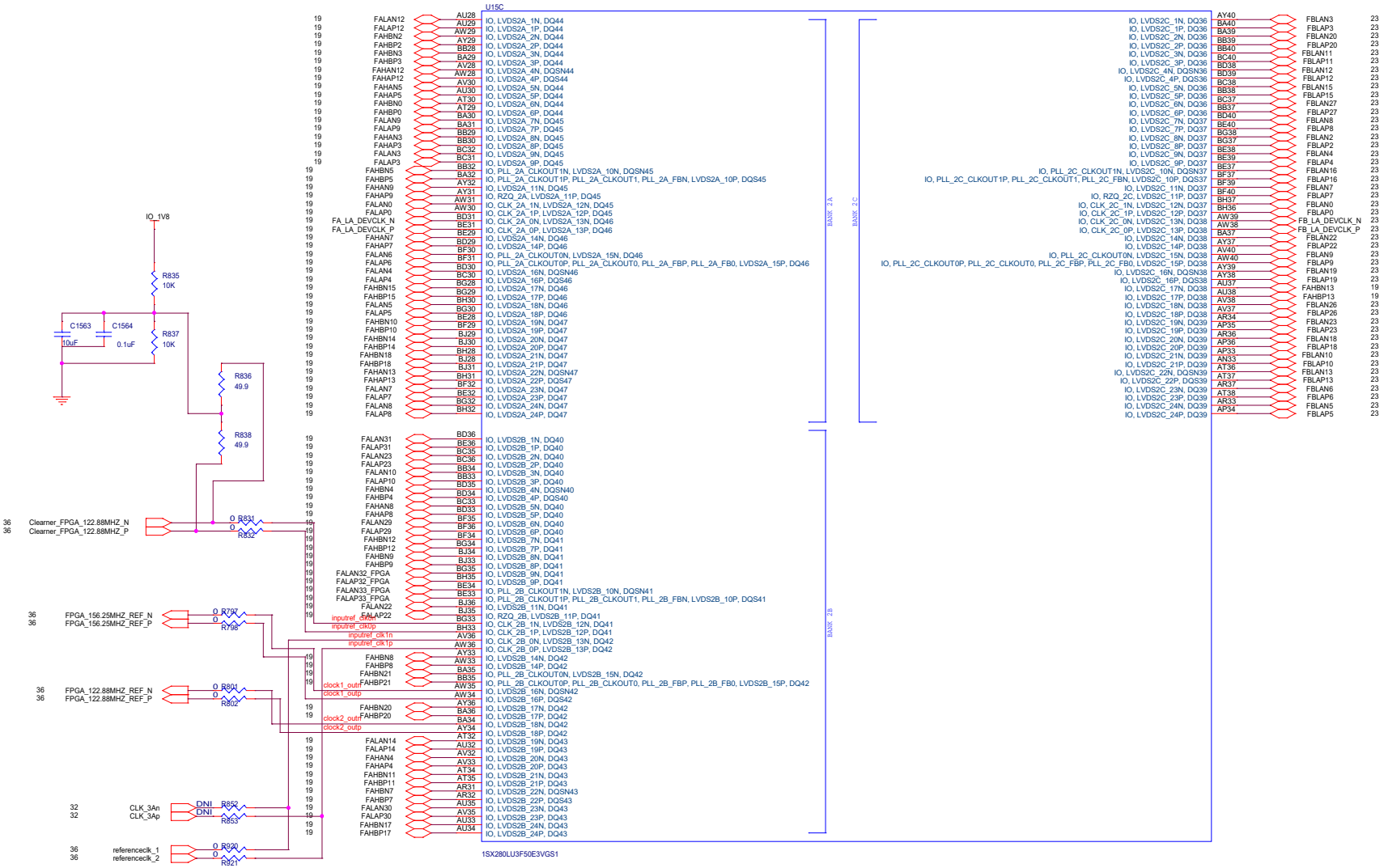
Stratix 10 Banks 2 A/B/C



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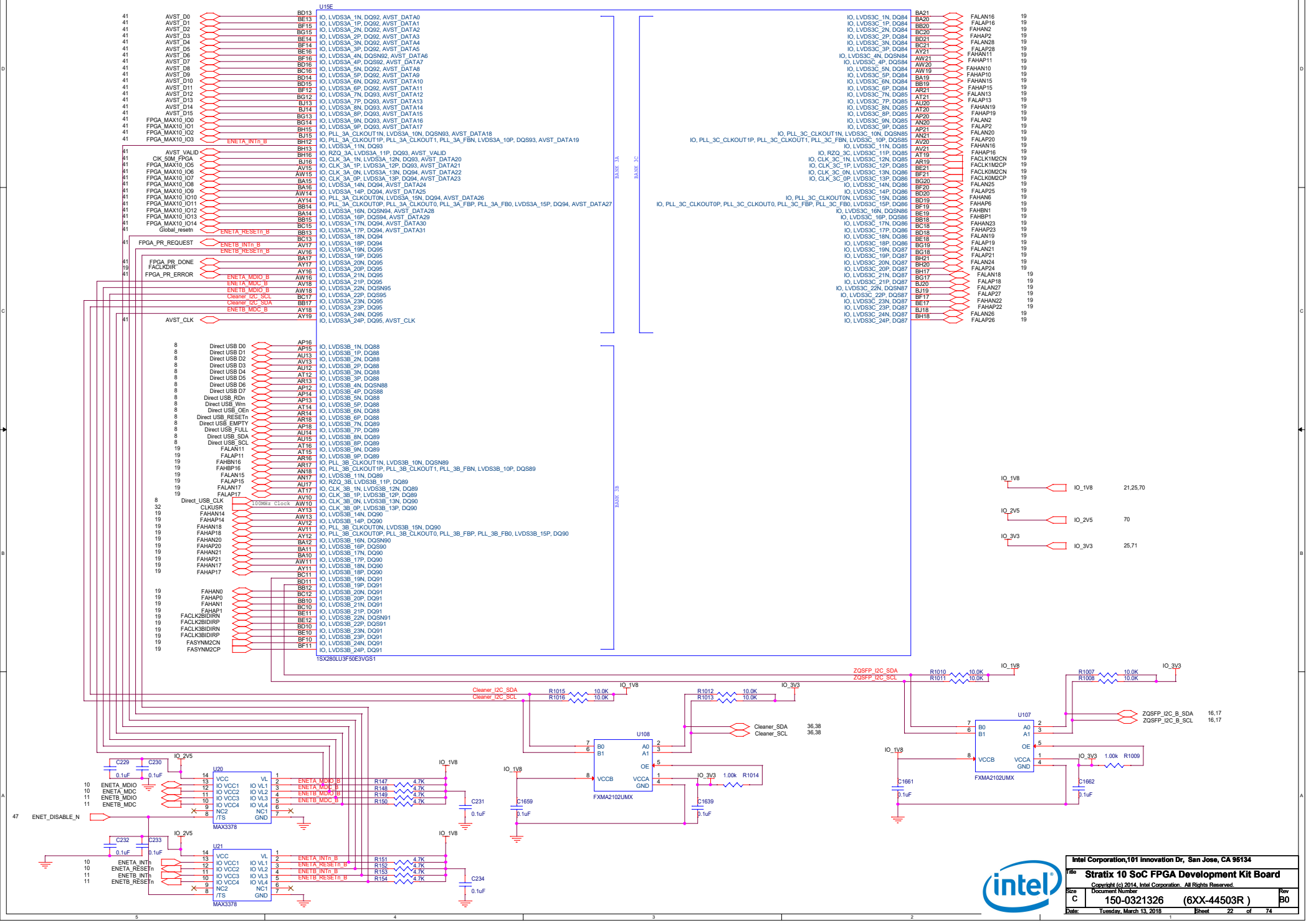
Stratix 10 Banks - 3 A/B/C



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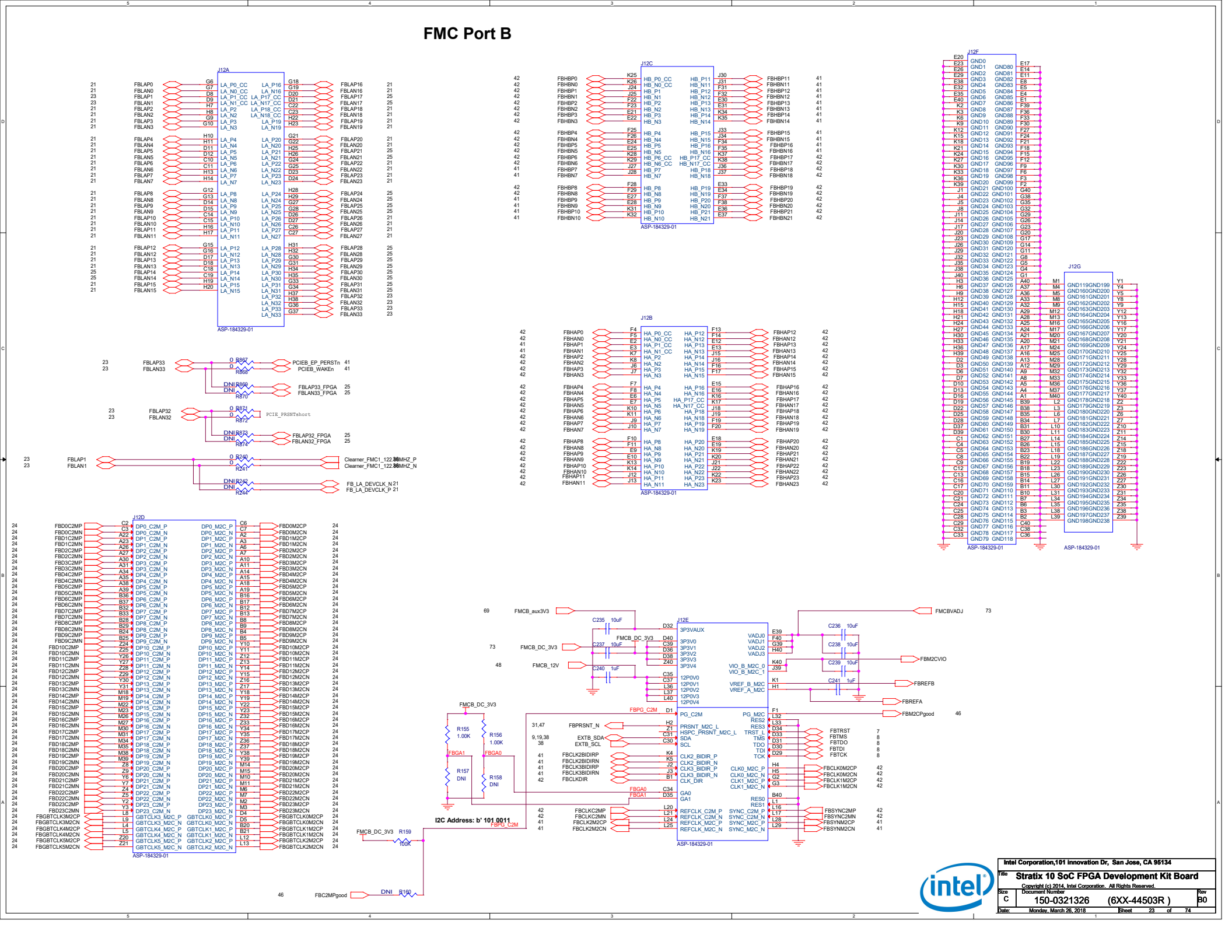
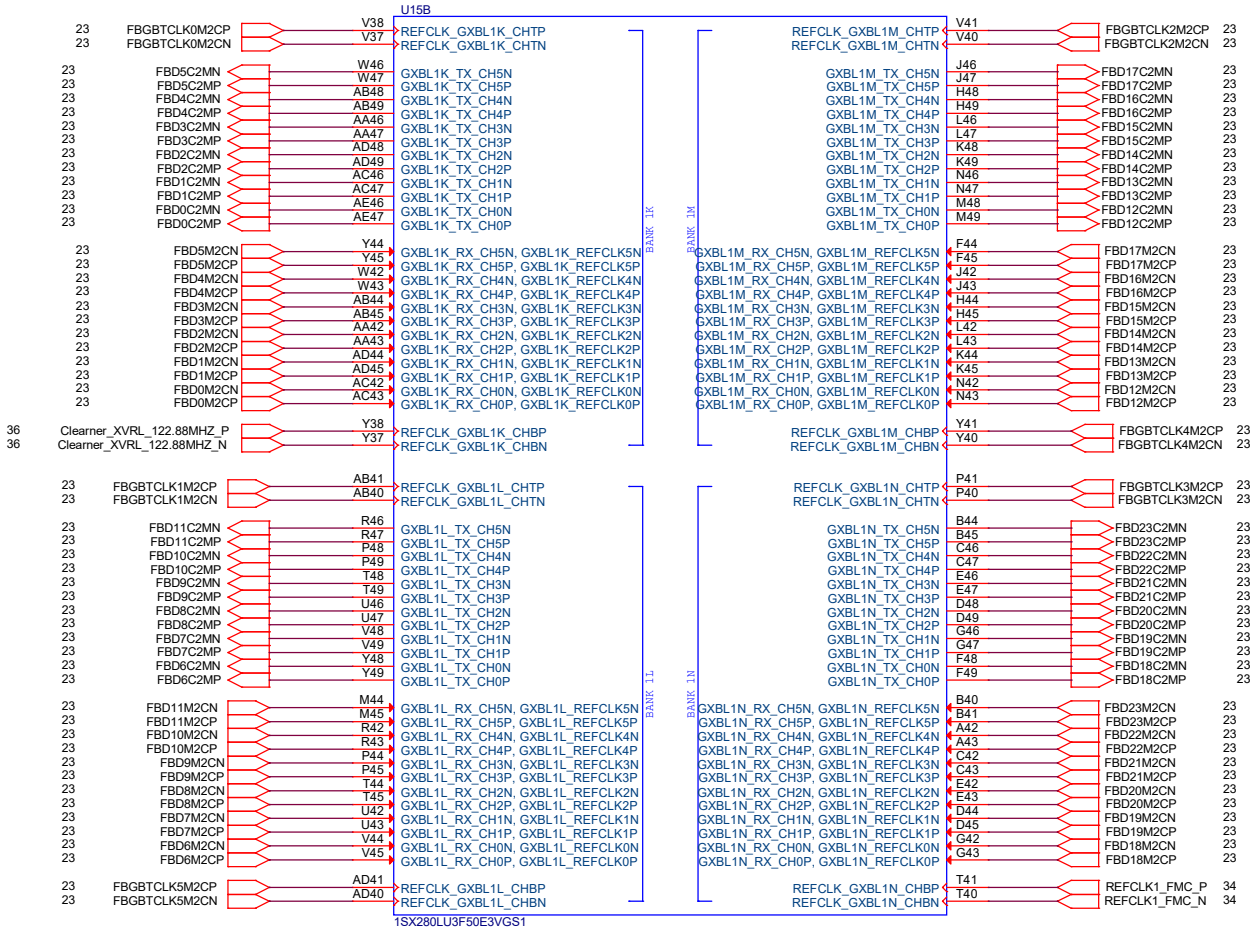
FMC Port B



Stratix 10 XCVR Banks - 1K/L/M/N



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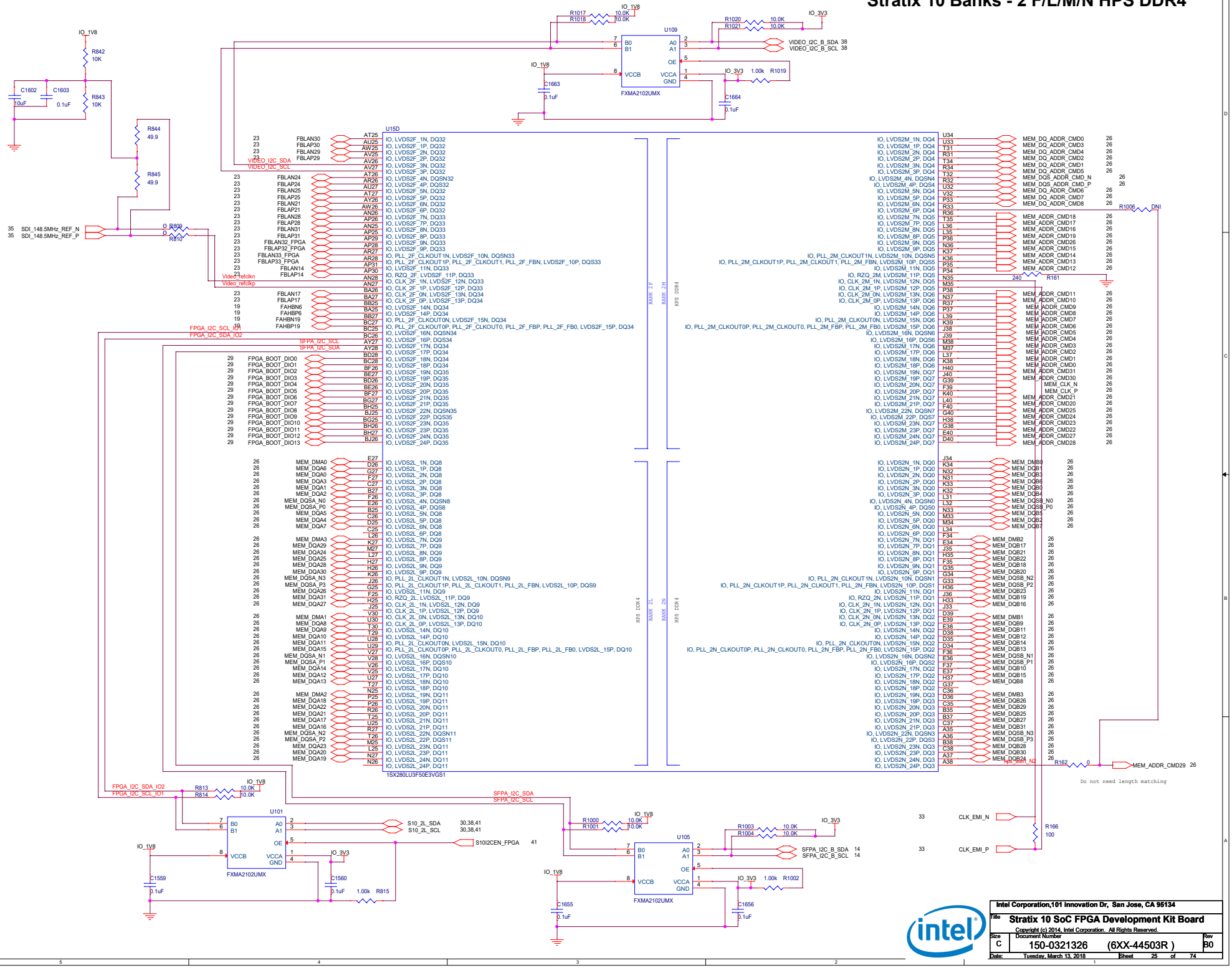
Stratix 10 Banks - 2 F/L/M/N HPS DDR4



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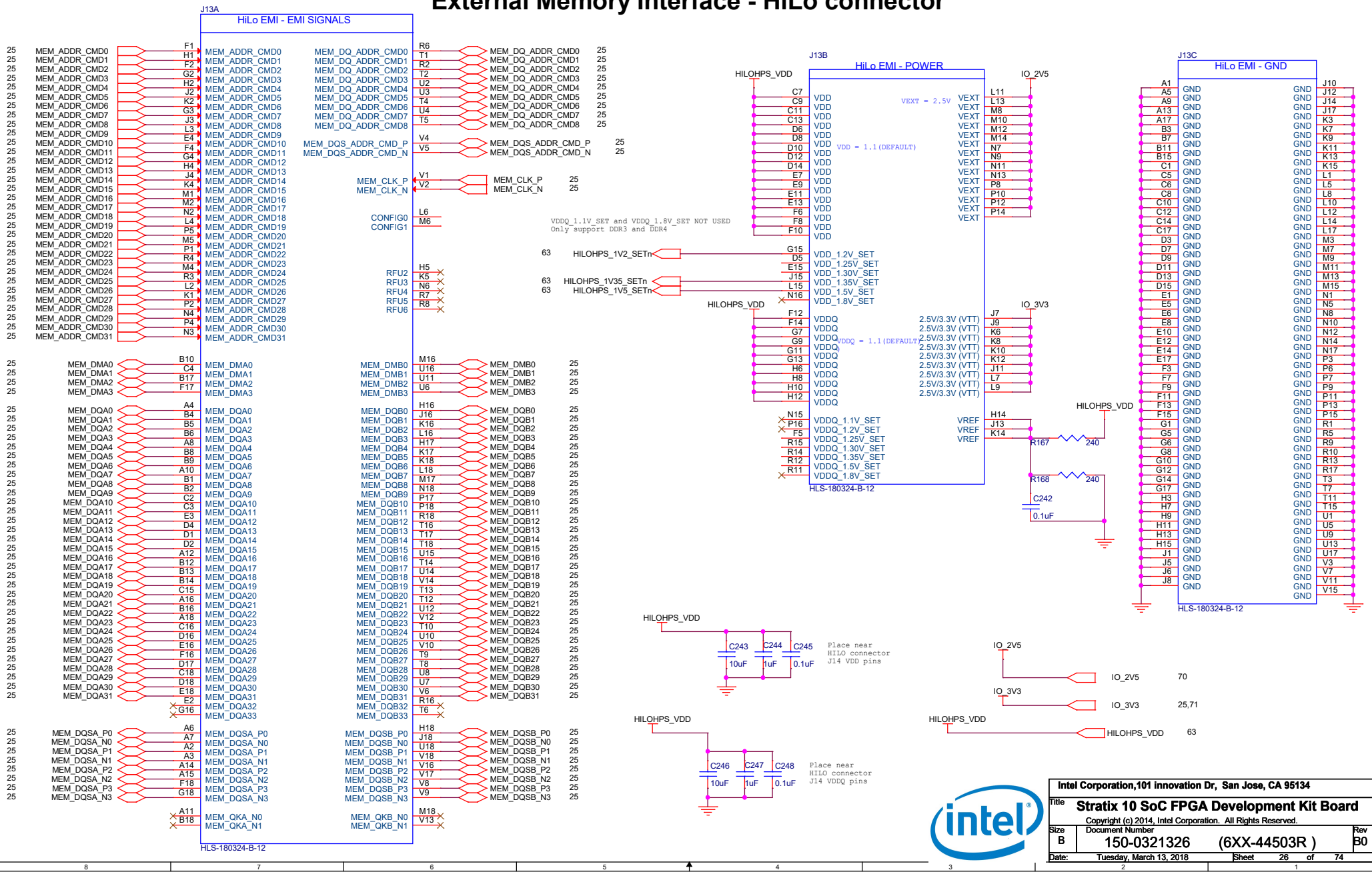
External Memory Interface - HiLo connector



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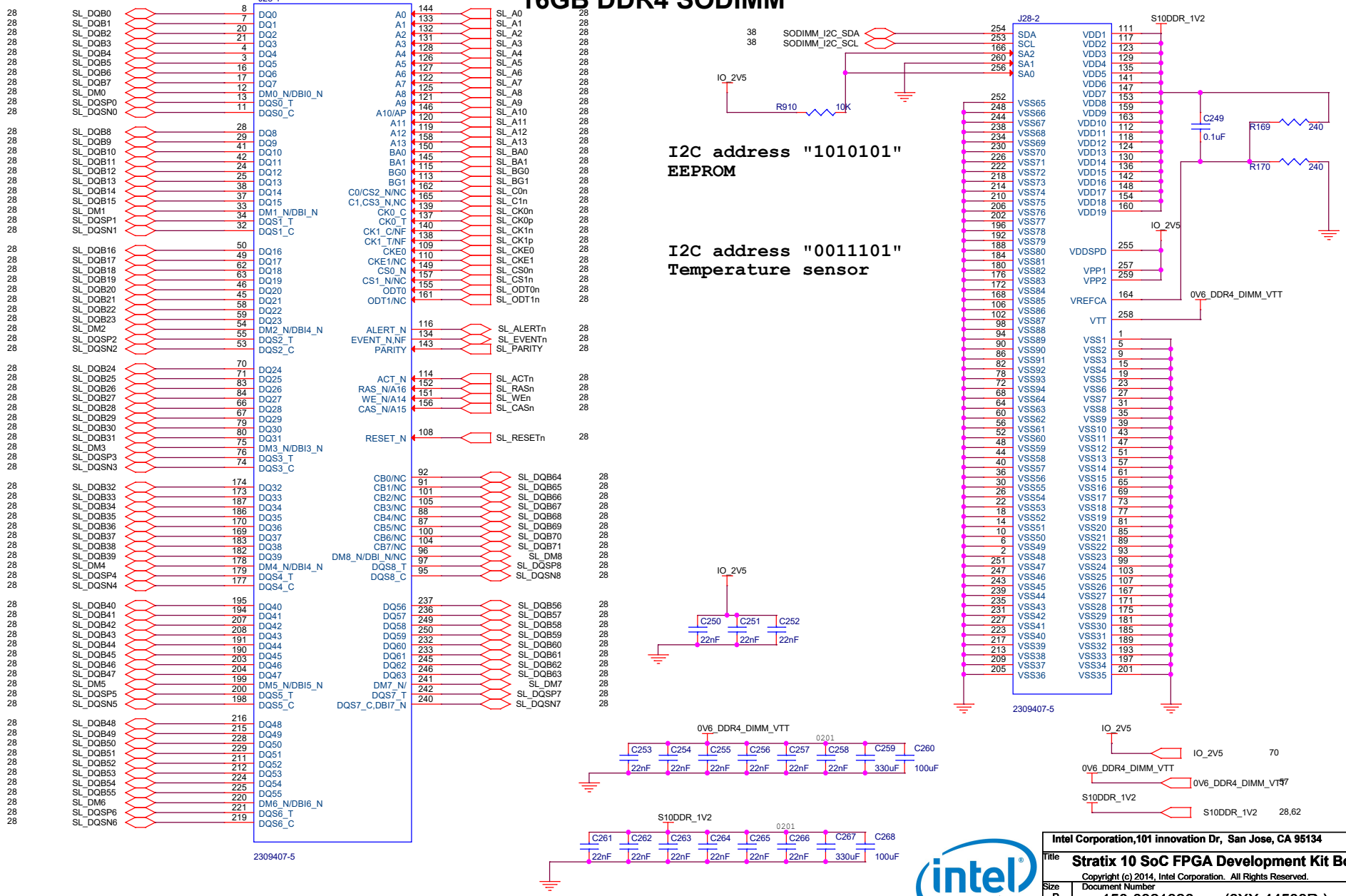
16GB DDR4 SODIMM



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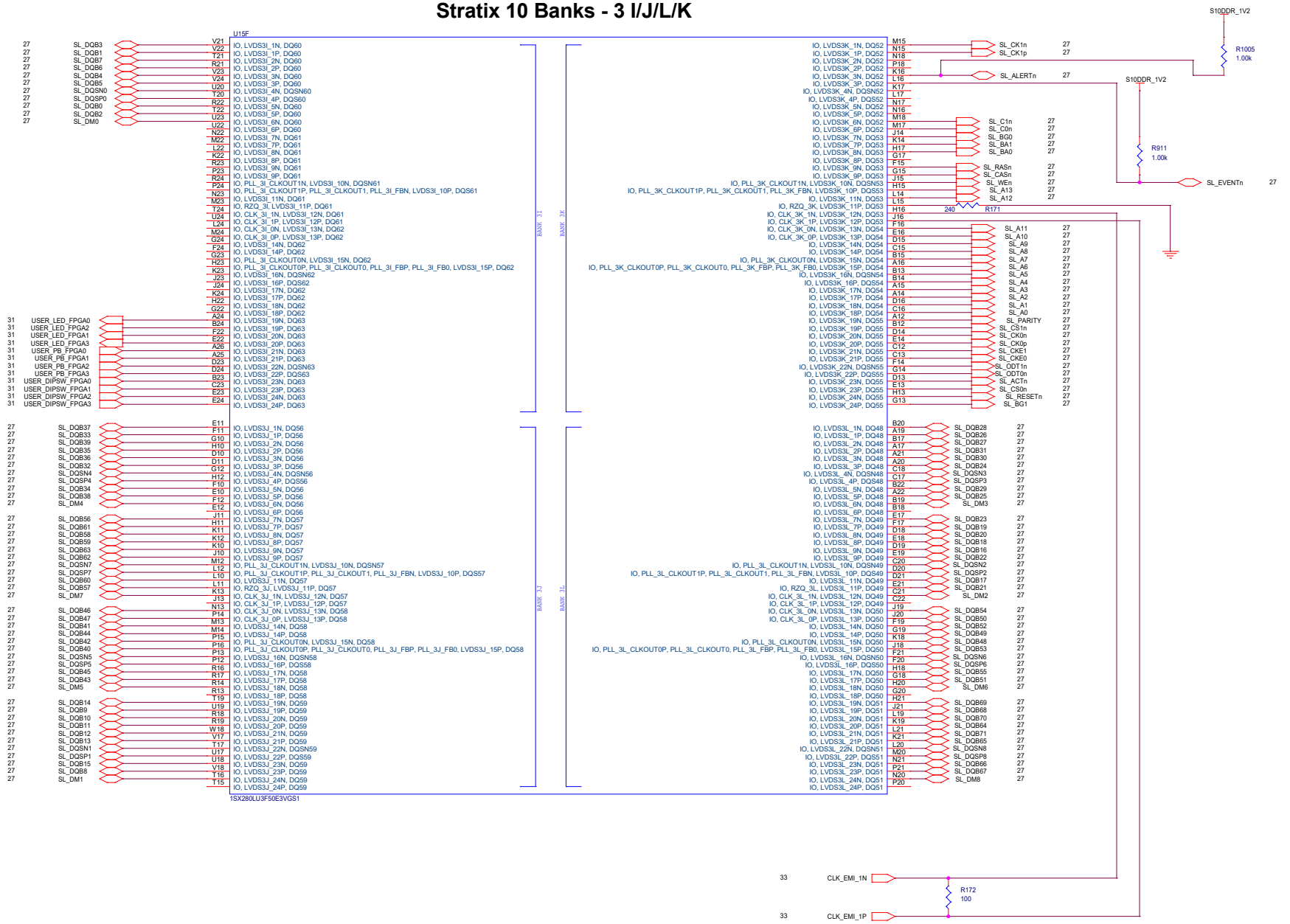
Stratix 10 Banks - 3 I/J/L/K



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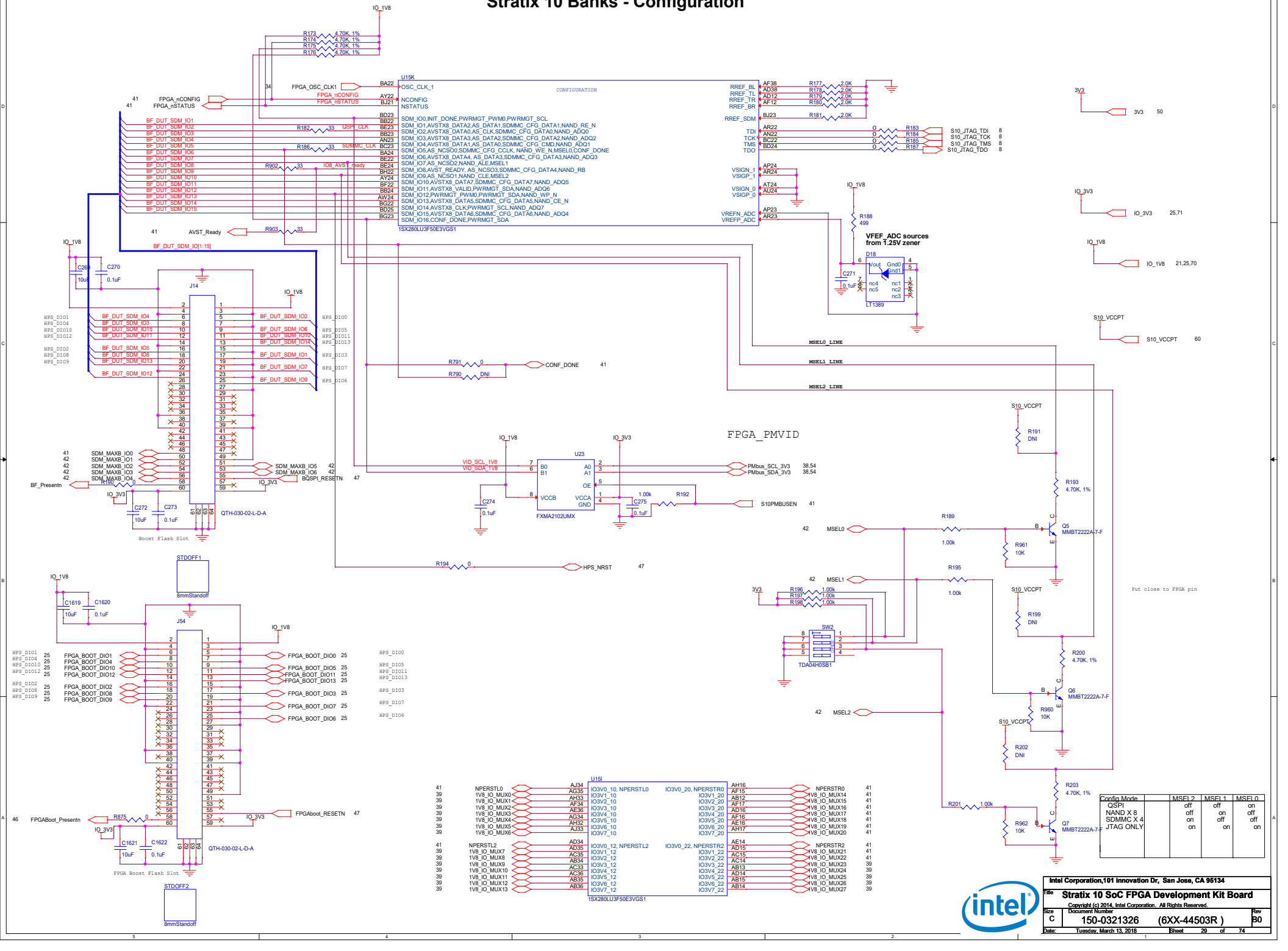
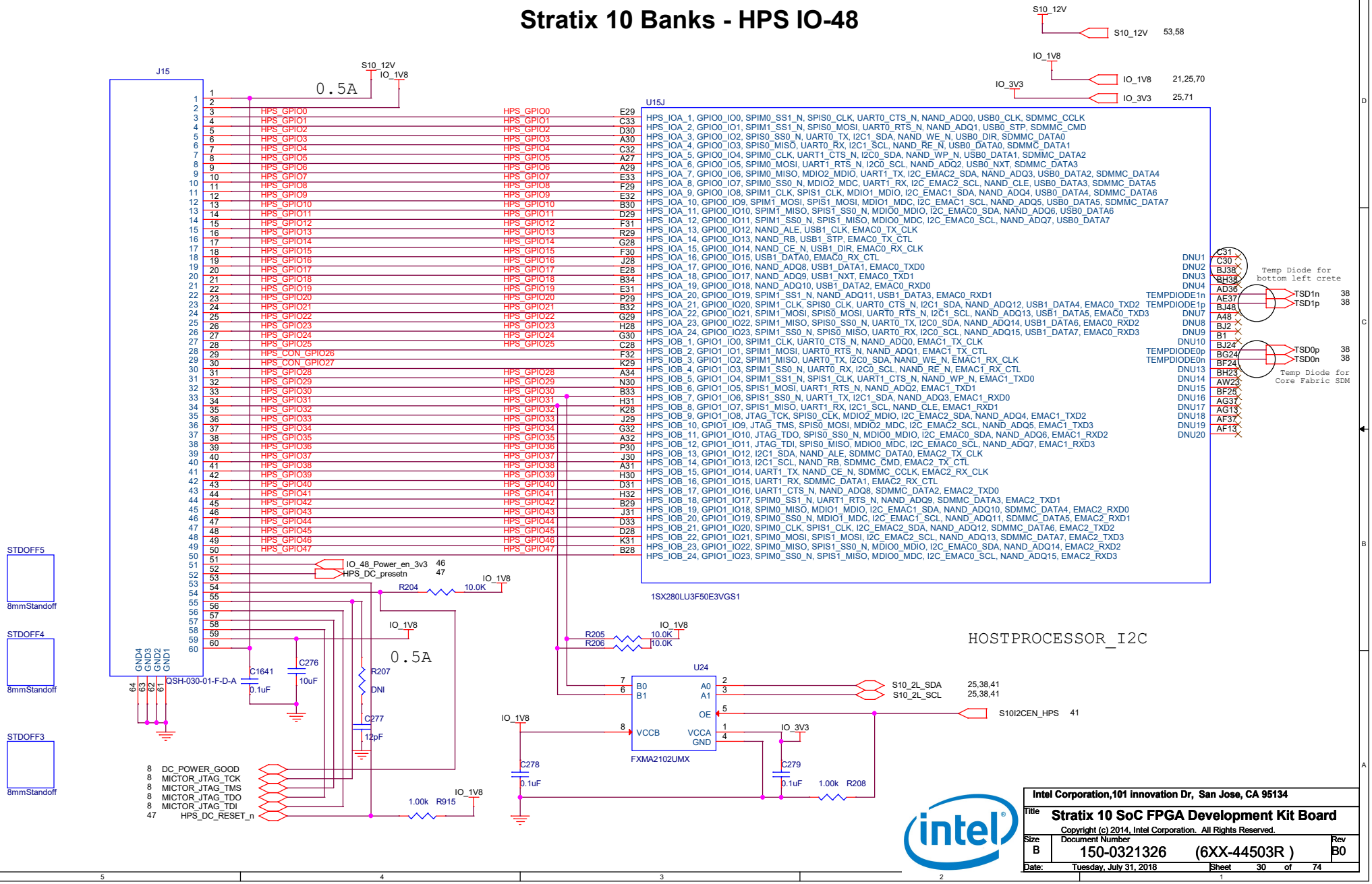
Stratix 10 Banks - Configuration



Stratix 10 Banks - HPS IO-48



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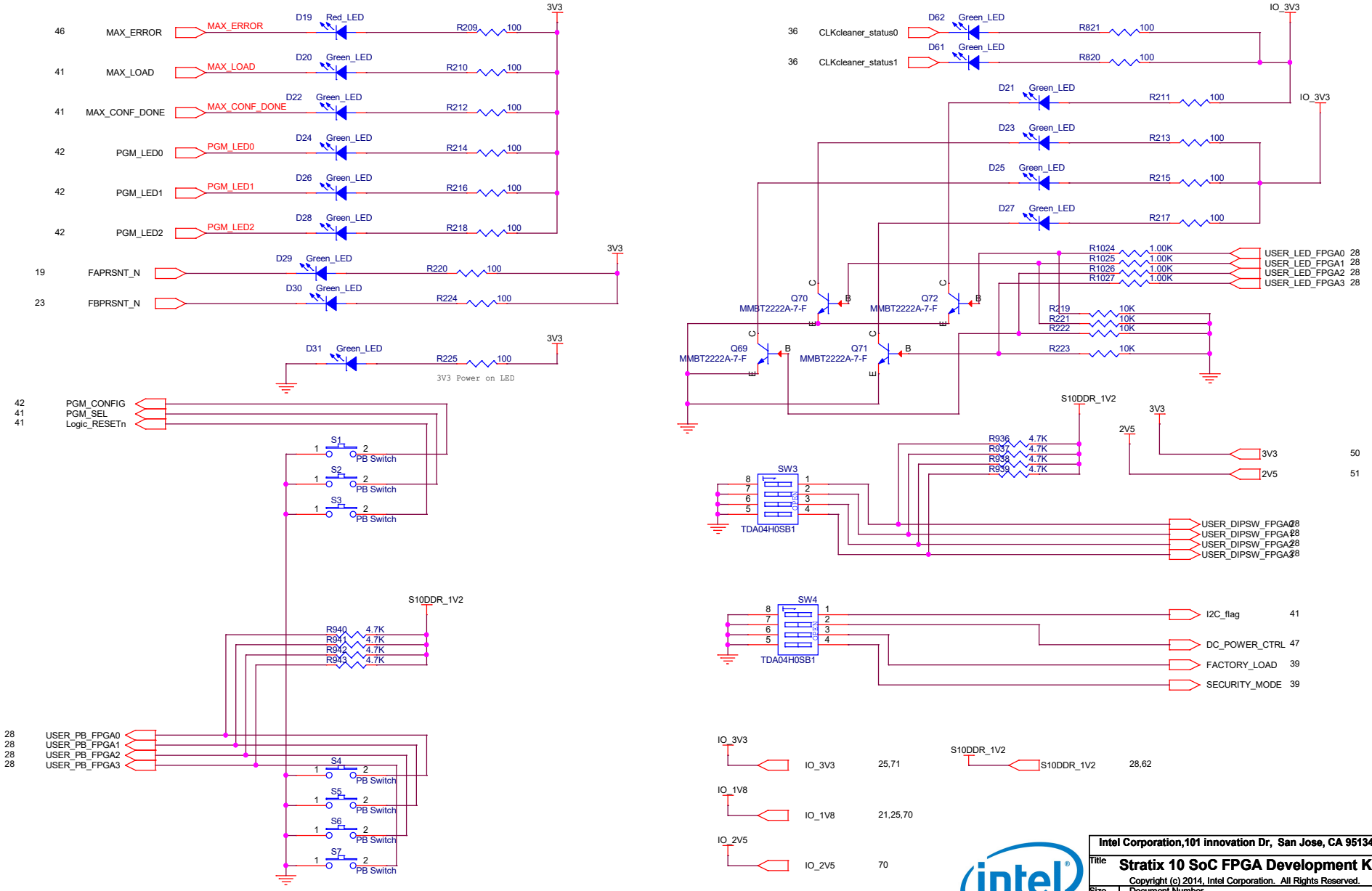
User I/O



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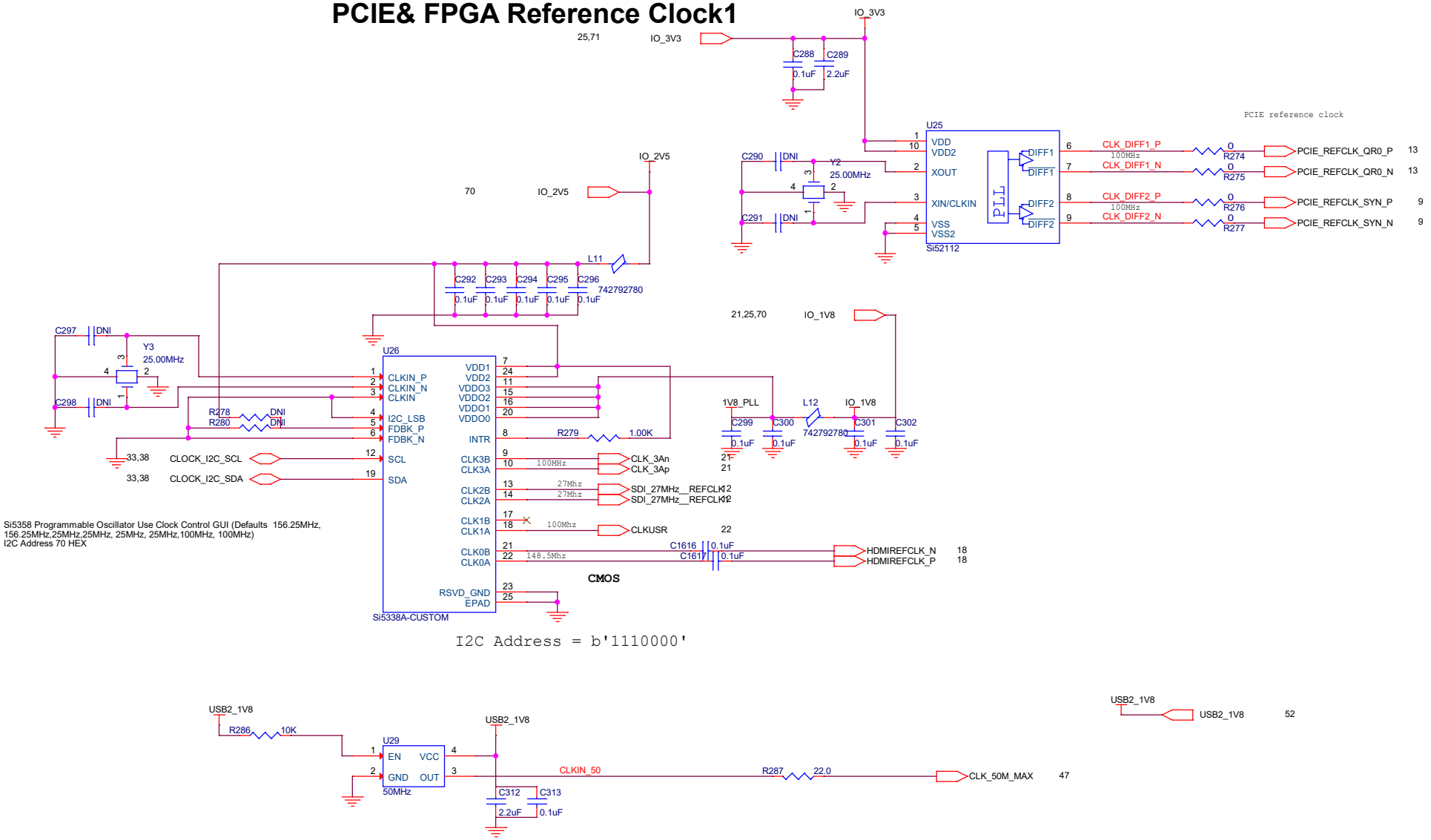
PCIE& FPGA Reference Clock1



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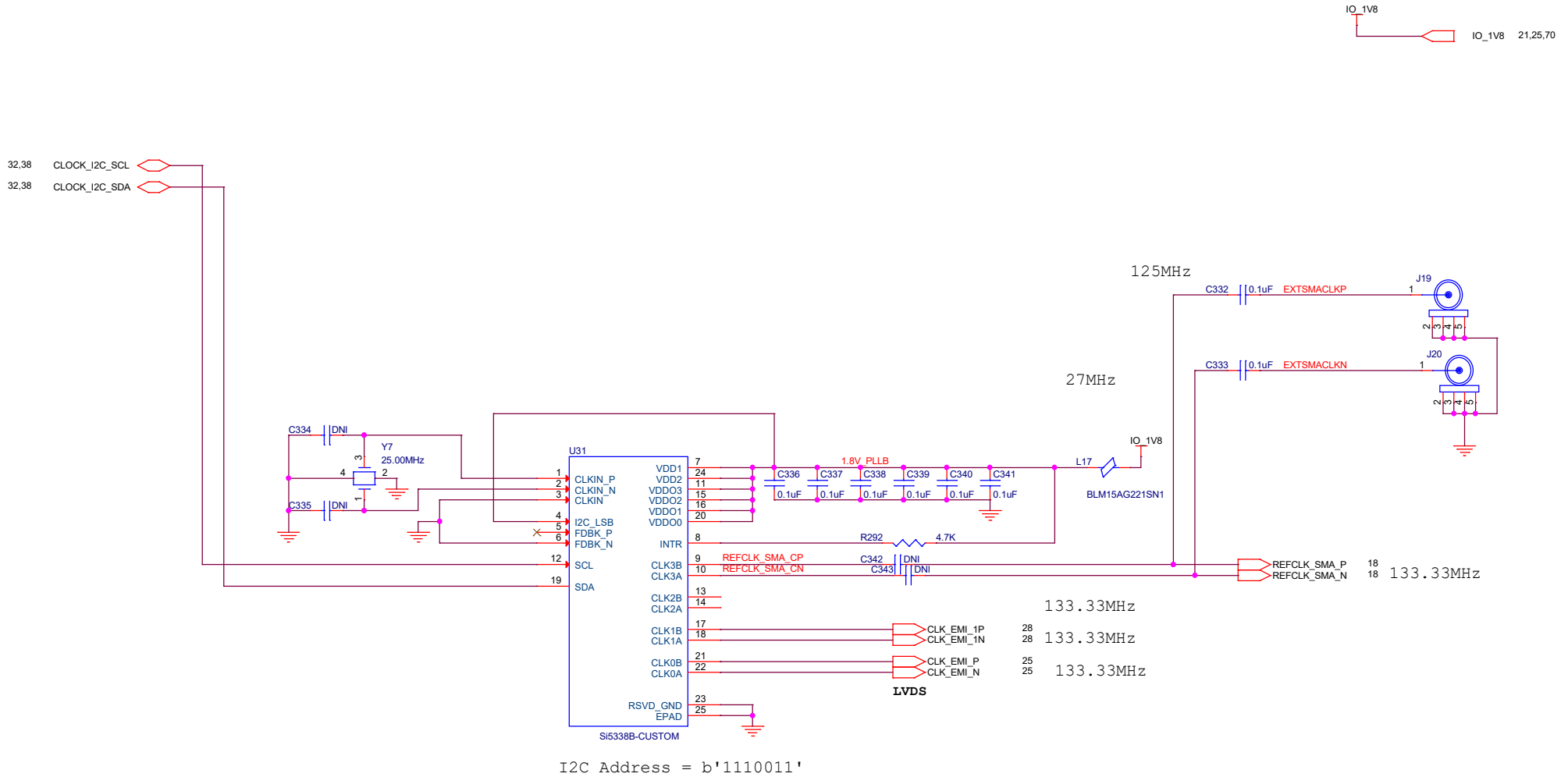
FPGA Memomory Reference clock



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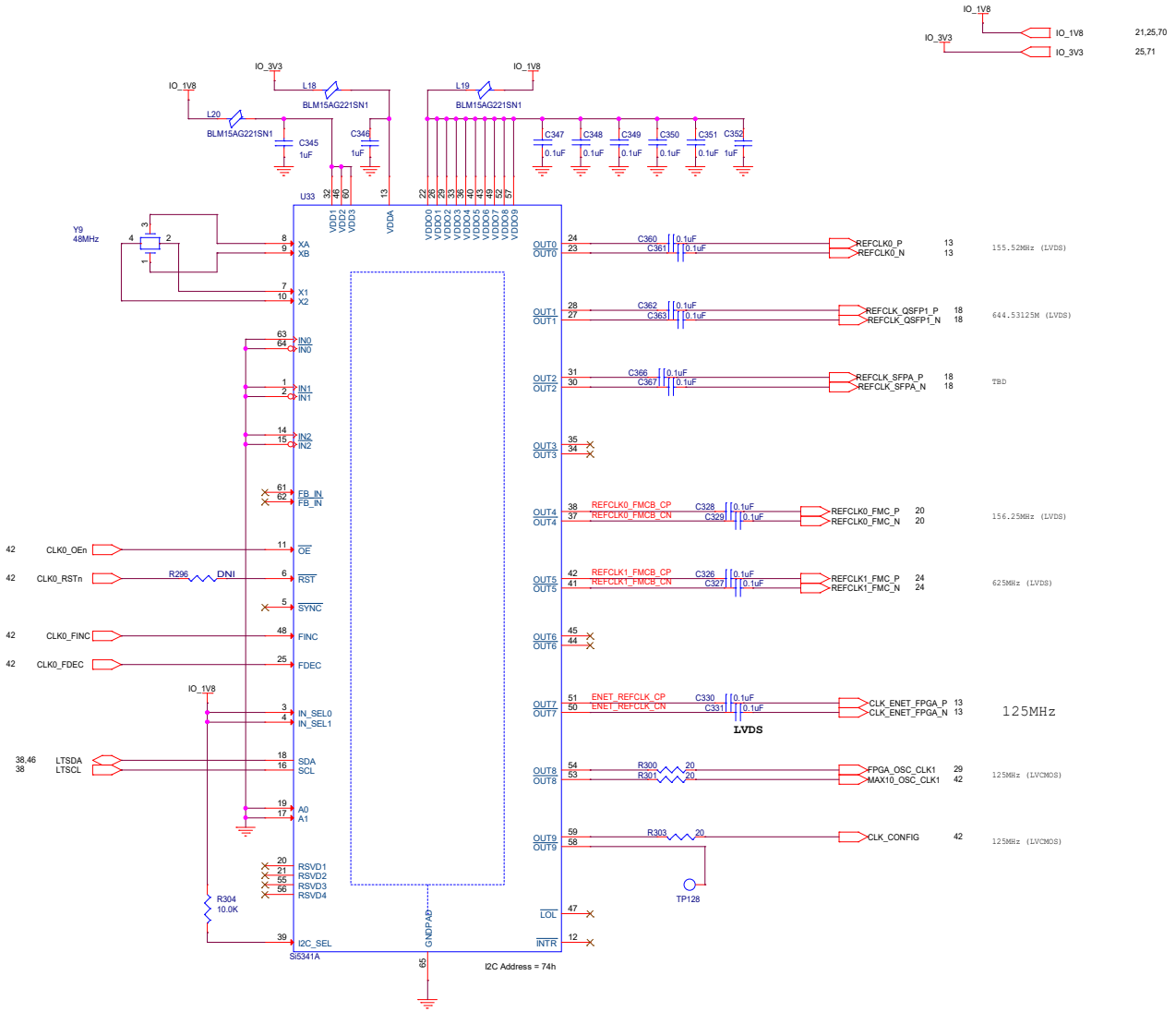
FPGA Transceiver reference Clocks



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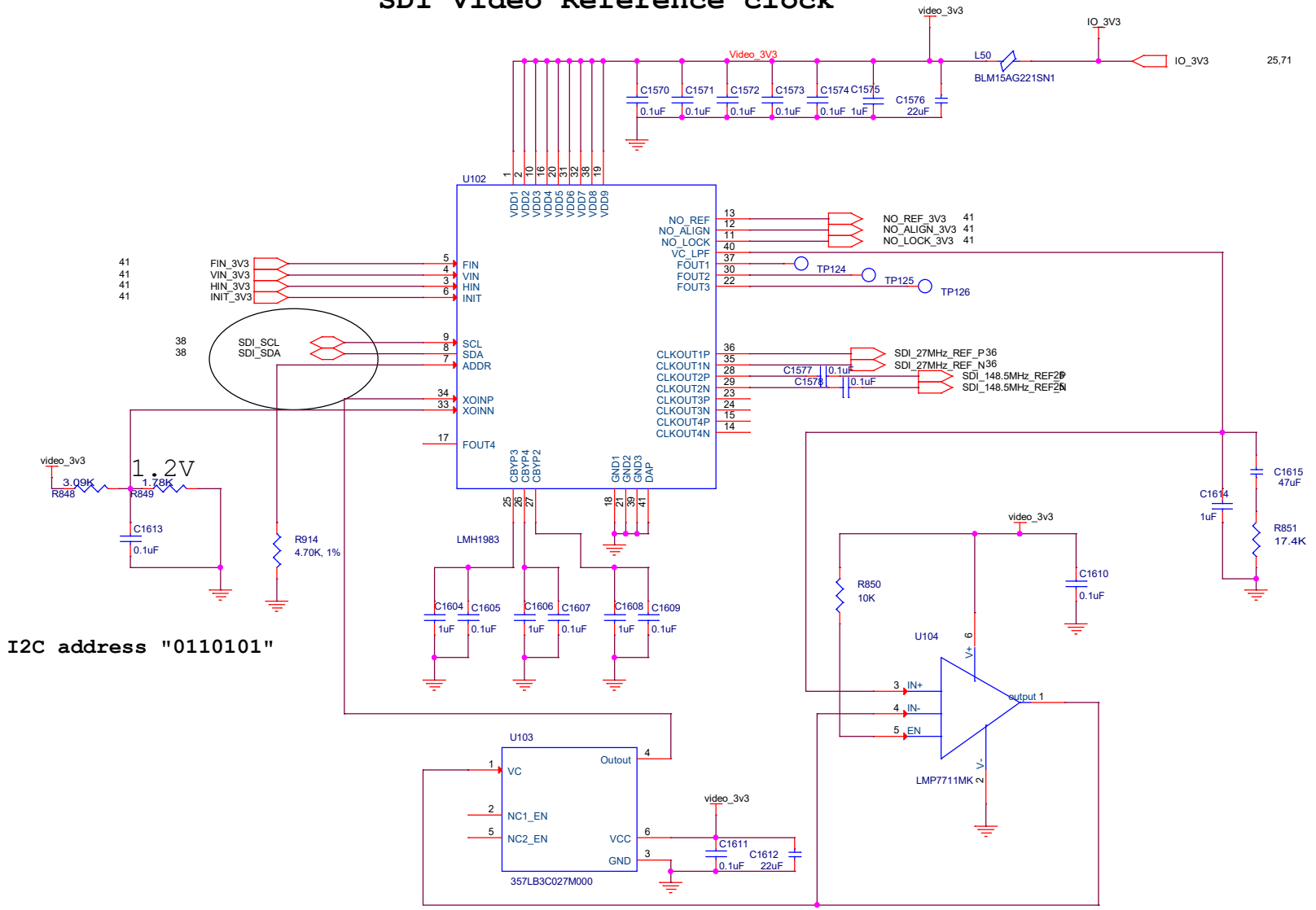
SDI Video Reference clock



I2C address "0110101"

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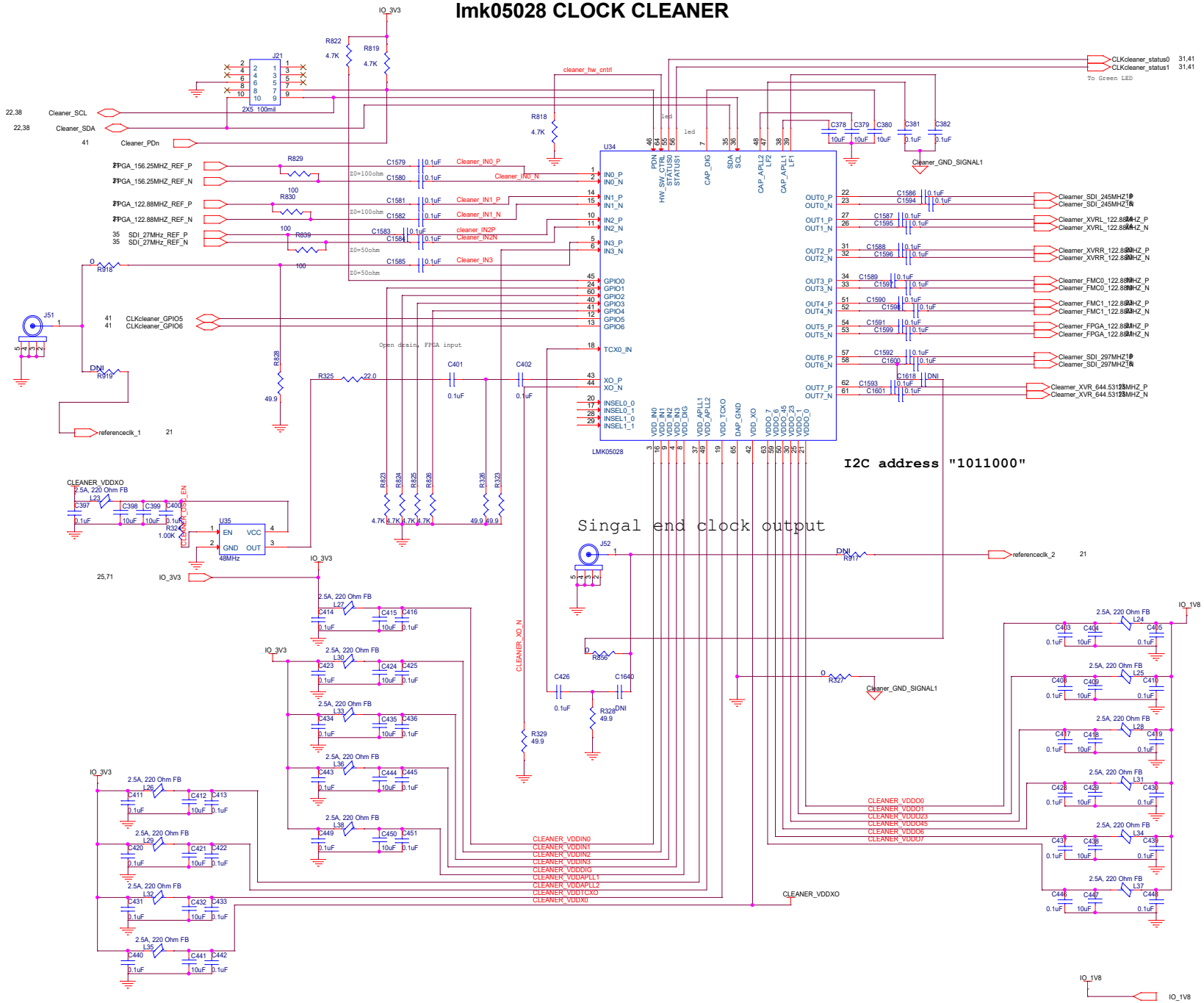
lmk05028 CLOCK CLEANER



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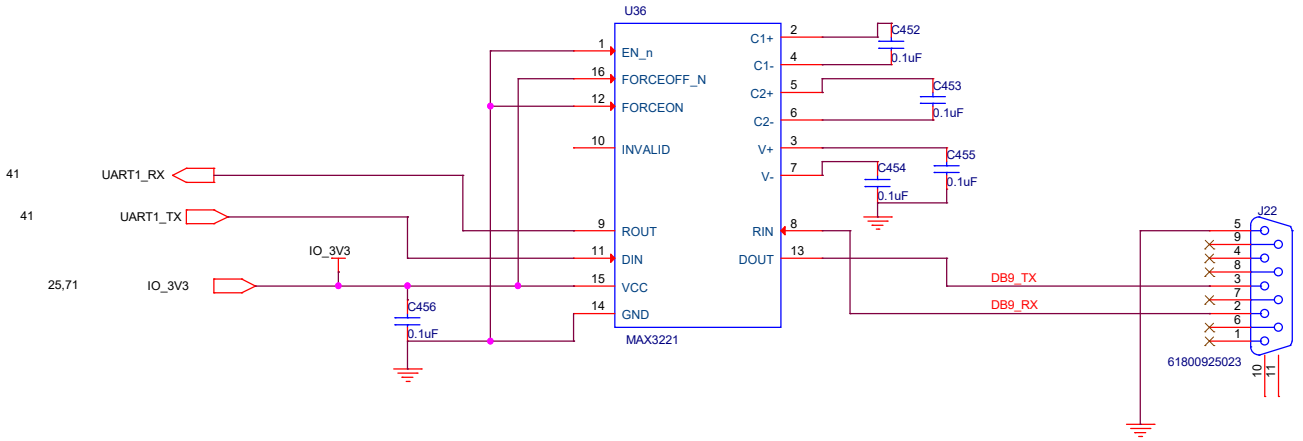
UART Port B



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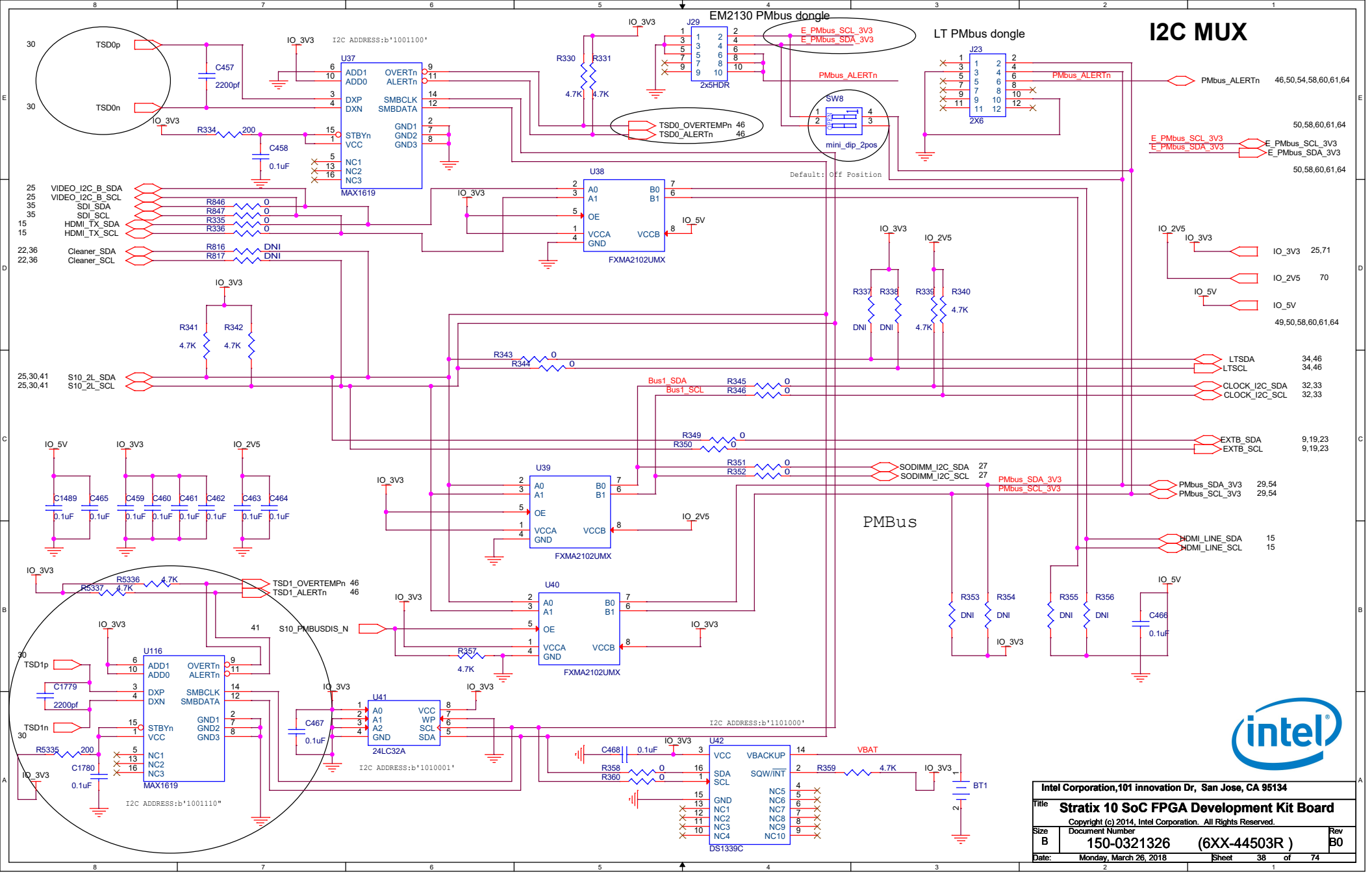
I2C MUX
EM2130 PMbus dongle
LT PMbus dongle
PMBus
TSD0p
TSD0n
C457
2200pf
C458
0.1uF
R334
200
U37
MAX1619
I2C ADDRESS:b'1001100'
ADD1
ADD0
DXP
DXN
STBYn
VCC
SMBCLK
SMBDATA
GND1
GND2
GND3
NC1
NC2
NC3
OVERTn
ALERTn
R330
R331
4.7K
J29
2x5HDR
E_PMbus_SCL_3V3
E_PMbus_SDA_3V3
PMbus_ALERTn
TSD0_OVERTEMPn
TSD0_ALERTn
SW8
mini_dip_2pos
Default: Off Position
J23
2X6
VIDEO_I2C_B_SDA
VIDEO_I2C_B_SCL
SDI_SDA
SDI_SCL
HDMI_TX_SDA
HDMI_TX_SCL
Cleaner_SDA
Cleaner_SCL
R846
R847
R335
R336
R816
R817
DNI
U38
FXMA2102UMX
A0
A1
B0
B1
OE
VCCA
VCCB
GND
IO_3V3
IO_5V
IO_2V5
R337
R338
R339
R340
R341
R342
S10_2L_SDA
S10_2L_SCL
R343
R344
Bus1_SDA
Bus1_SCL
R345
R346
R349
R350
R351
R352
U39
U40
R357
S10_PMBUSDIS_N
SODIMM_I2C_SDA
SODIMM_I2C_SCL
PMbus_SDA_3V3
PMbus_SCL_3V3
LTSDA
LTSCL
CLOCK_I2C_SDA
CLOCK_I2C_SCL
EXTB_SDA
EXTB_SCL
HDMI_LINE_SDA
HDMI_LINE_SCL
R353
R354
R355
R356
C466
C1489
C465
C459
C460
C461
C462
C463
C464
R5336
R5337
4.7K
TSD1_OVERTEMPn
TSD1_ALERTn
U116
TSD1p
TSD1n
C1779
C1780
R5335
200
I2C ADDRESS:b'1001110"
U41
24LC32A
I2C ADDRESS:b'1010001'
C467
I2C ADDRESS:b'1101000'
U42
DS1339C
VBACKUP
SQW/INT
SCL
SDA
NC5
NC6
NC7
NC8
NC9
NC10
C468
R358
R360
R359
VBAT
BT1
intel
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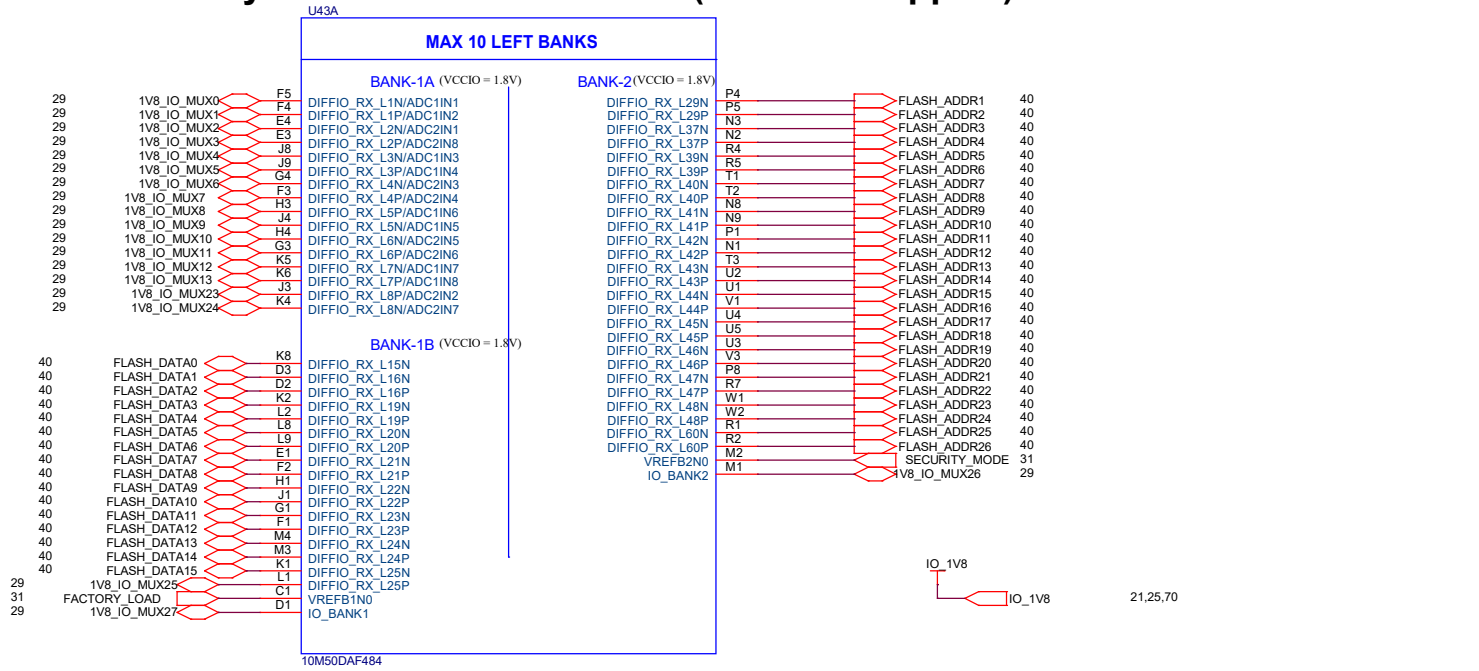
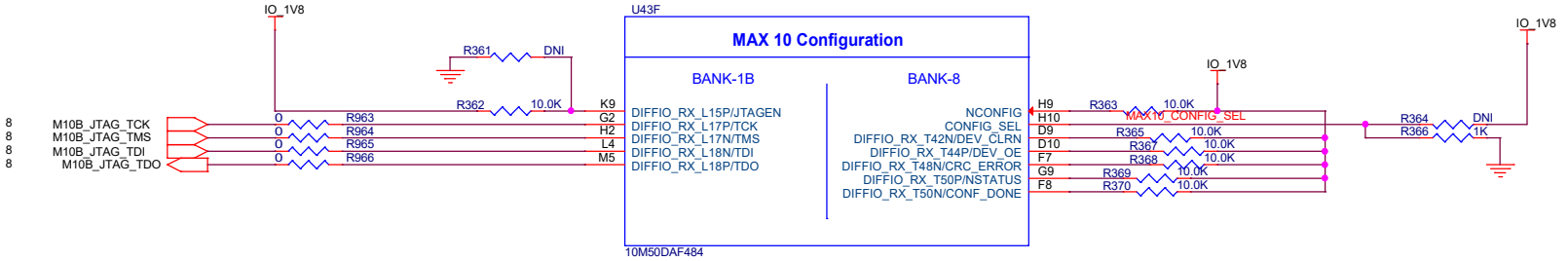
System MAX10 Controller (NO ADC Support)





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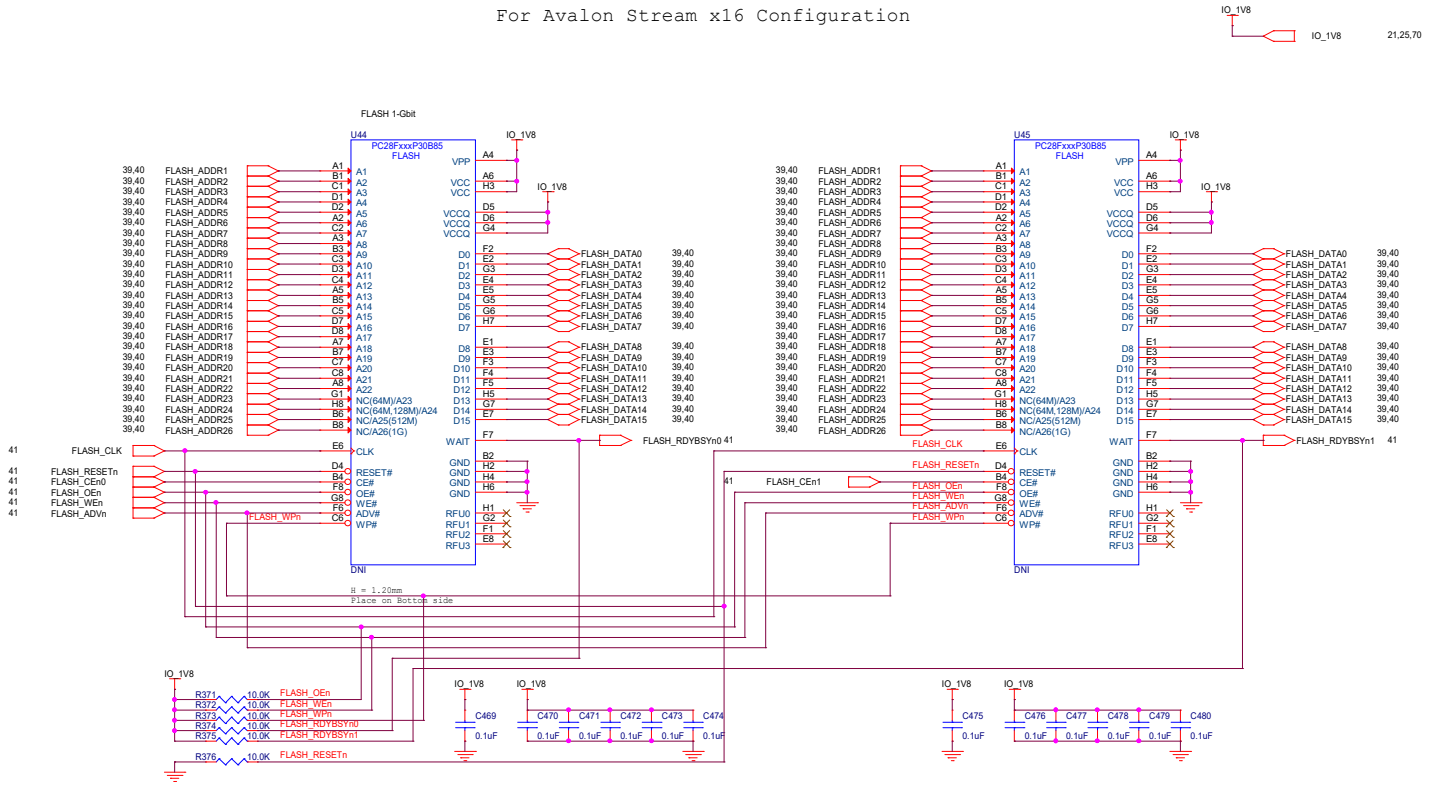
Flash Memory

For Avalon Stream x16 Configuration



- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.

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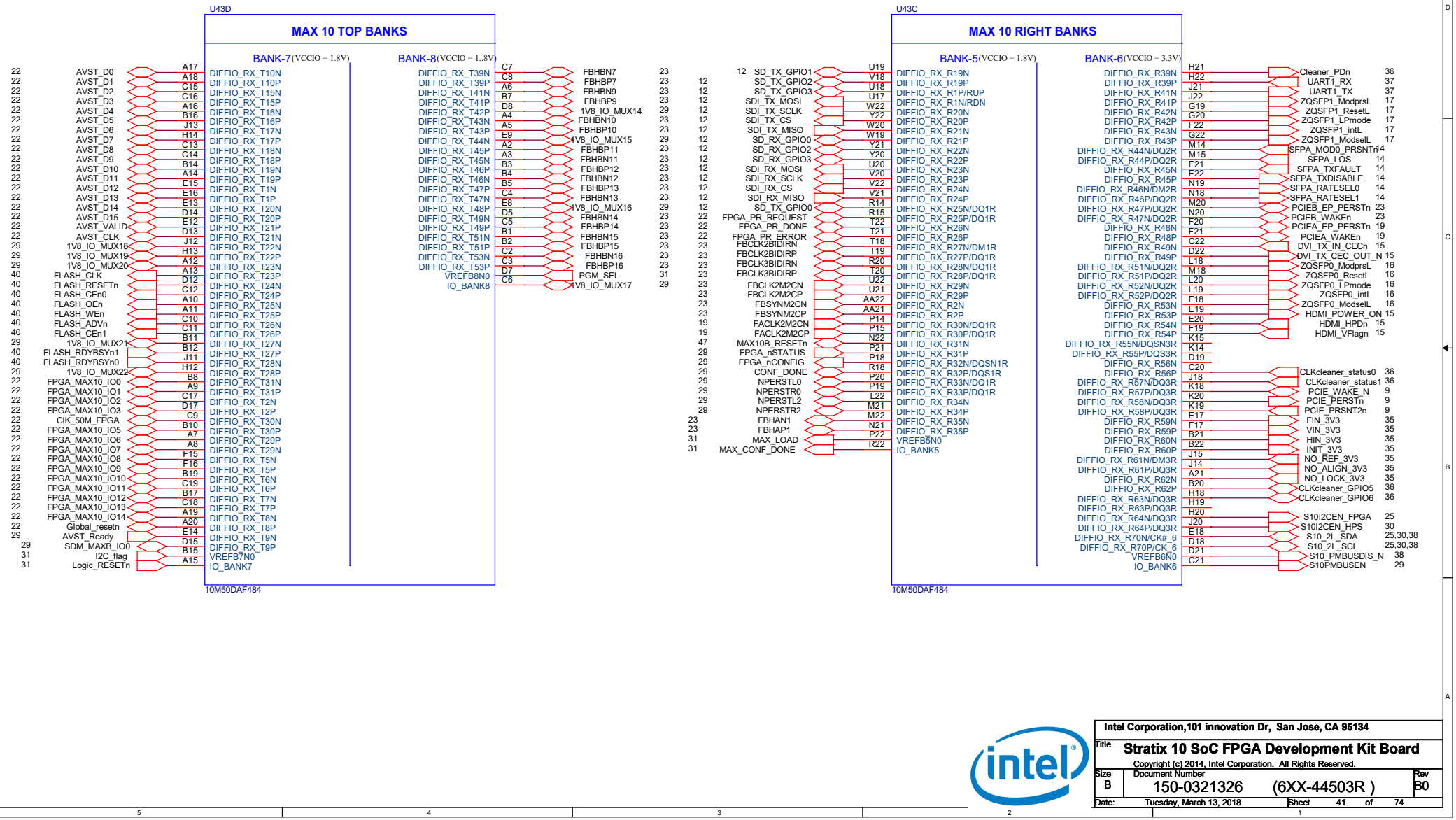
System MAX10 Controller 2



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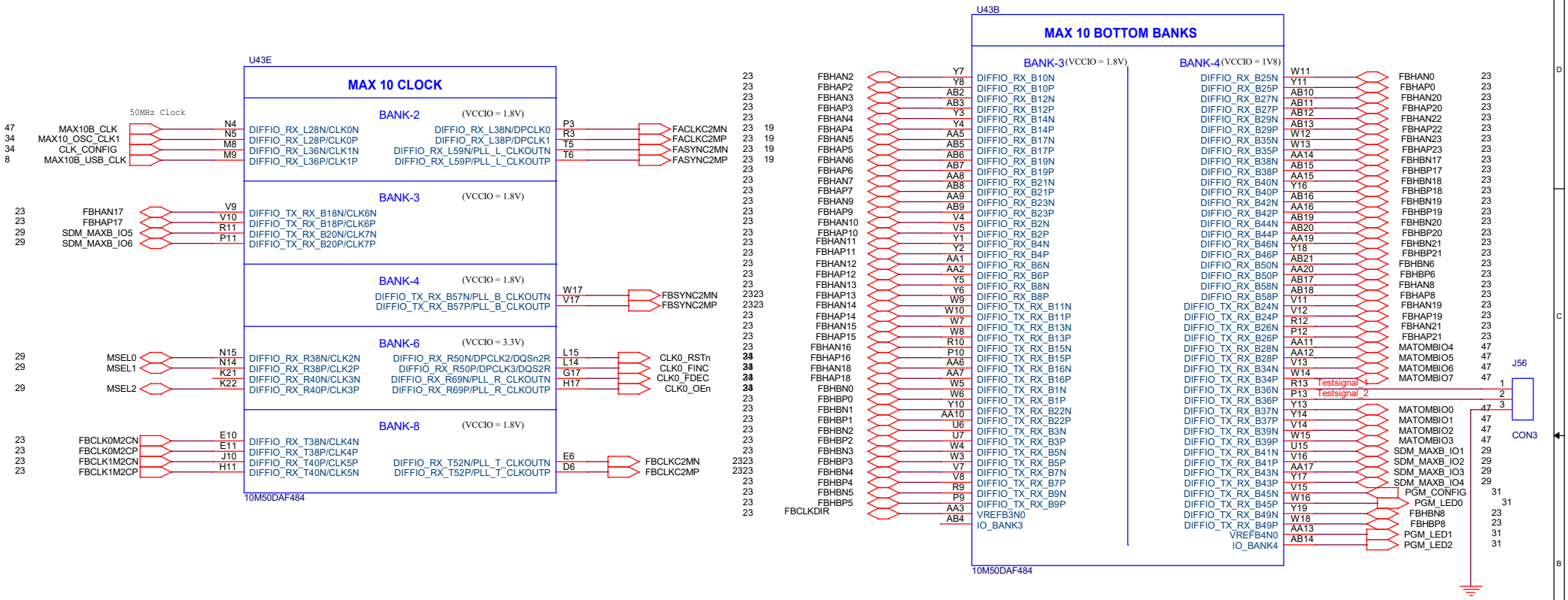
System MAX10 Controller 3



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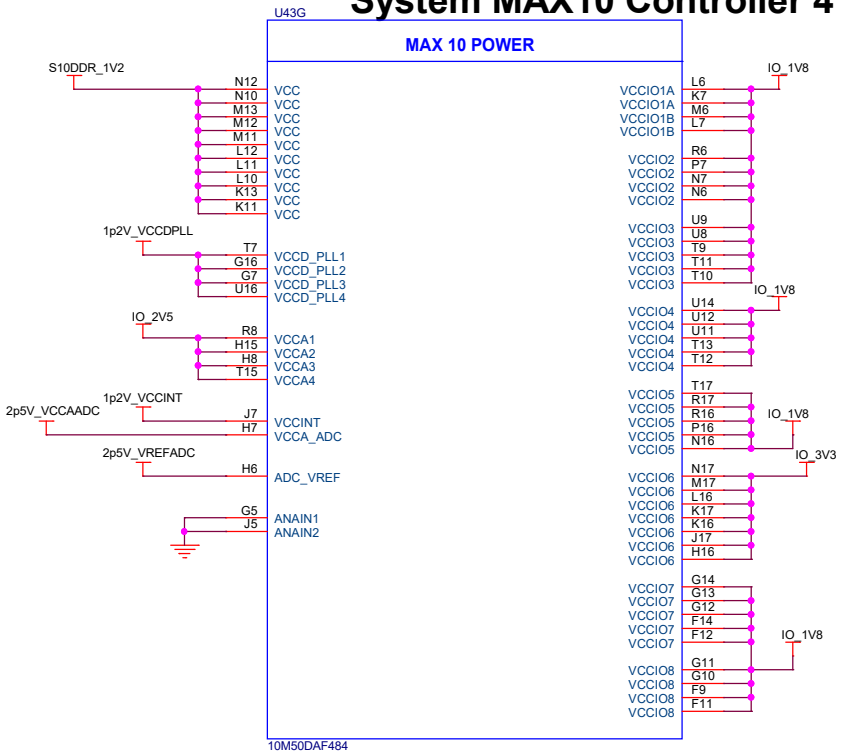
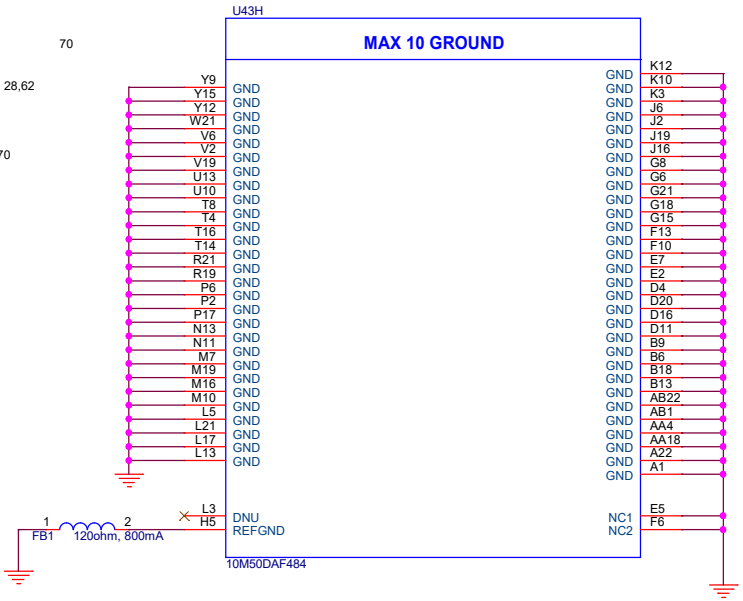
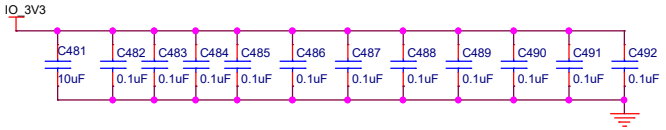
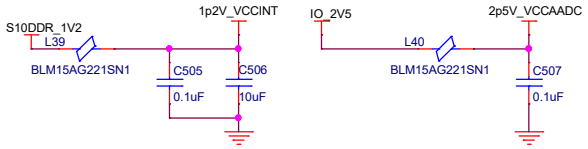
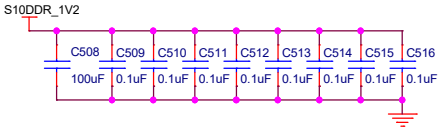
System MAX10 Controller 4

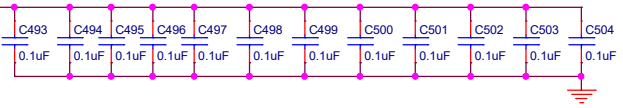


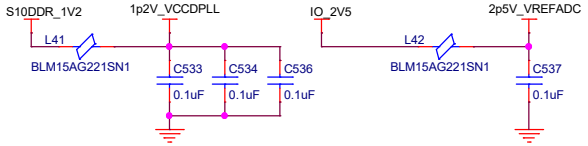


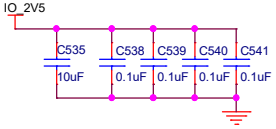


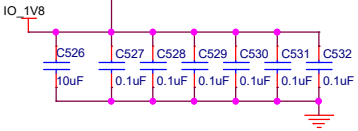


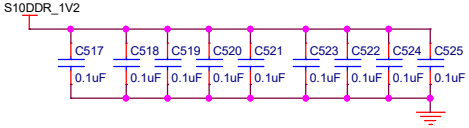


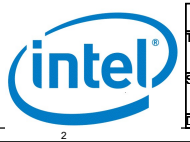












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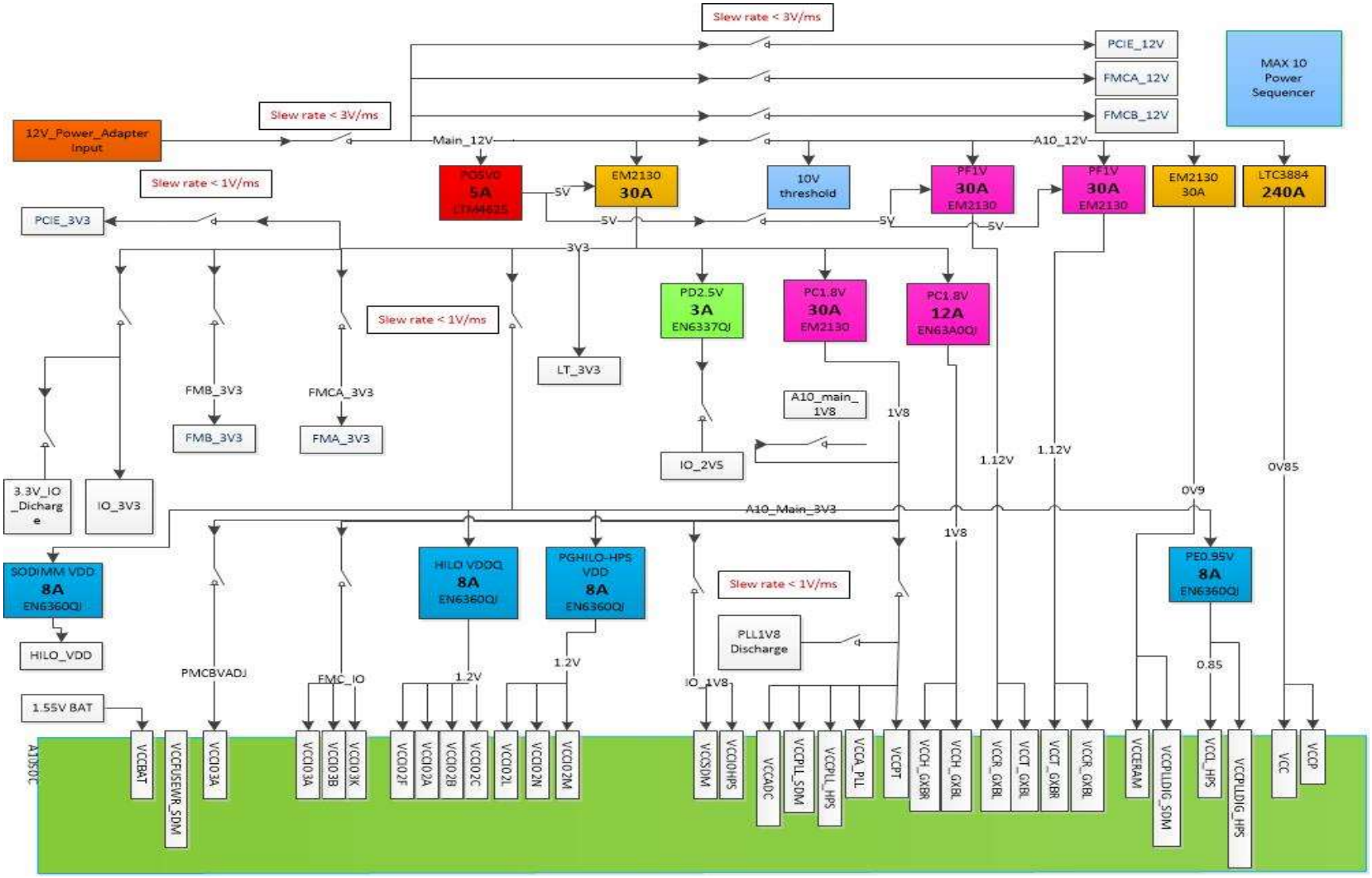
Stratix 10 SOC DEV KIT PDN Diagram



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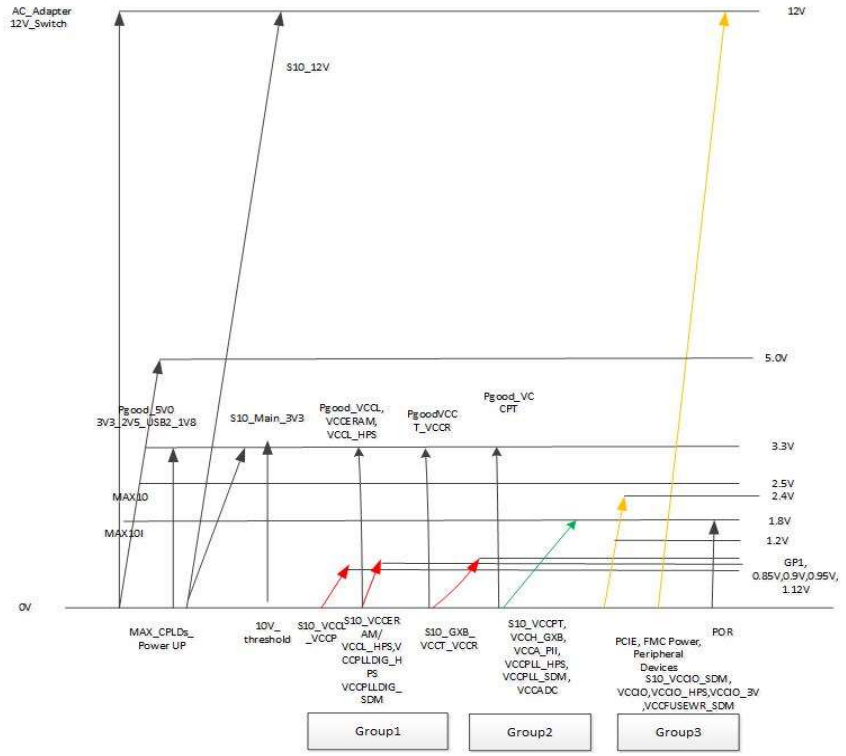
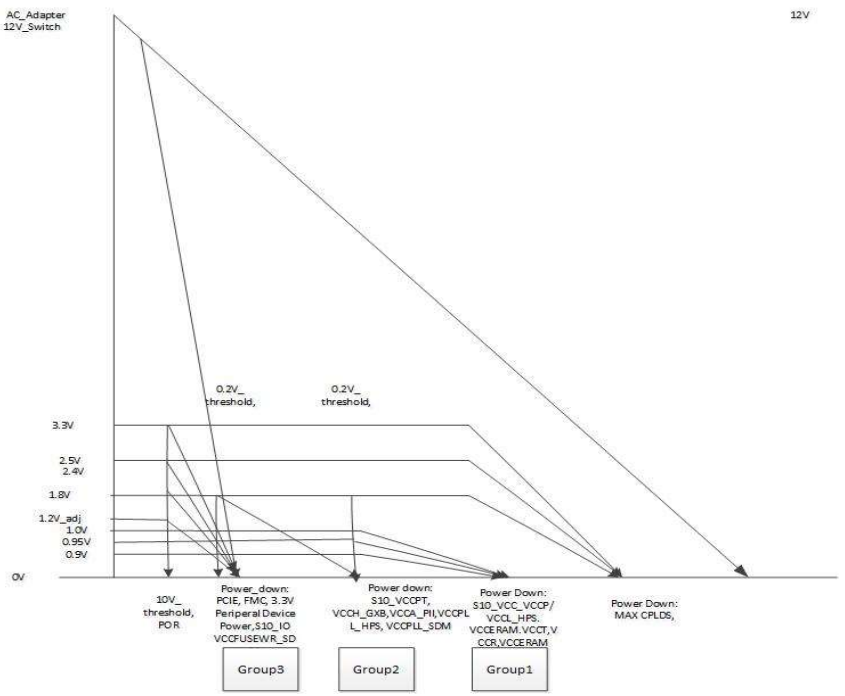
Stratix 10 SOC Power Sequence

S10 Dev KIT Power UP sequence



S10 Dev KIT Power Down sequence



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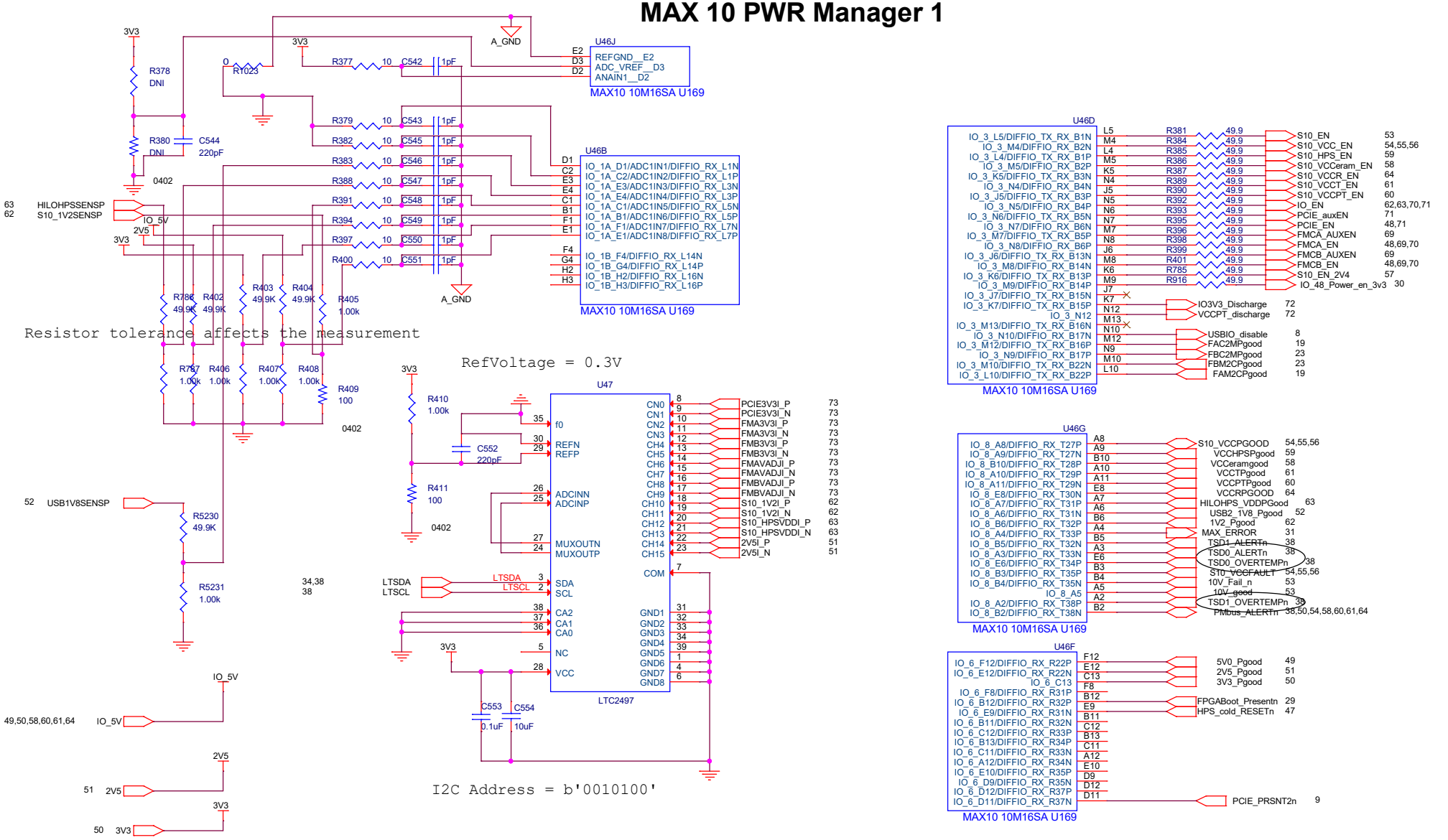
MAX 10 PWR Manager 1



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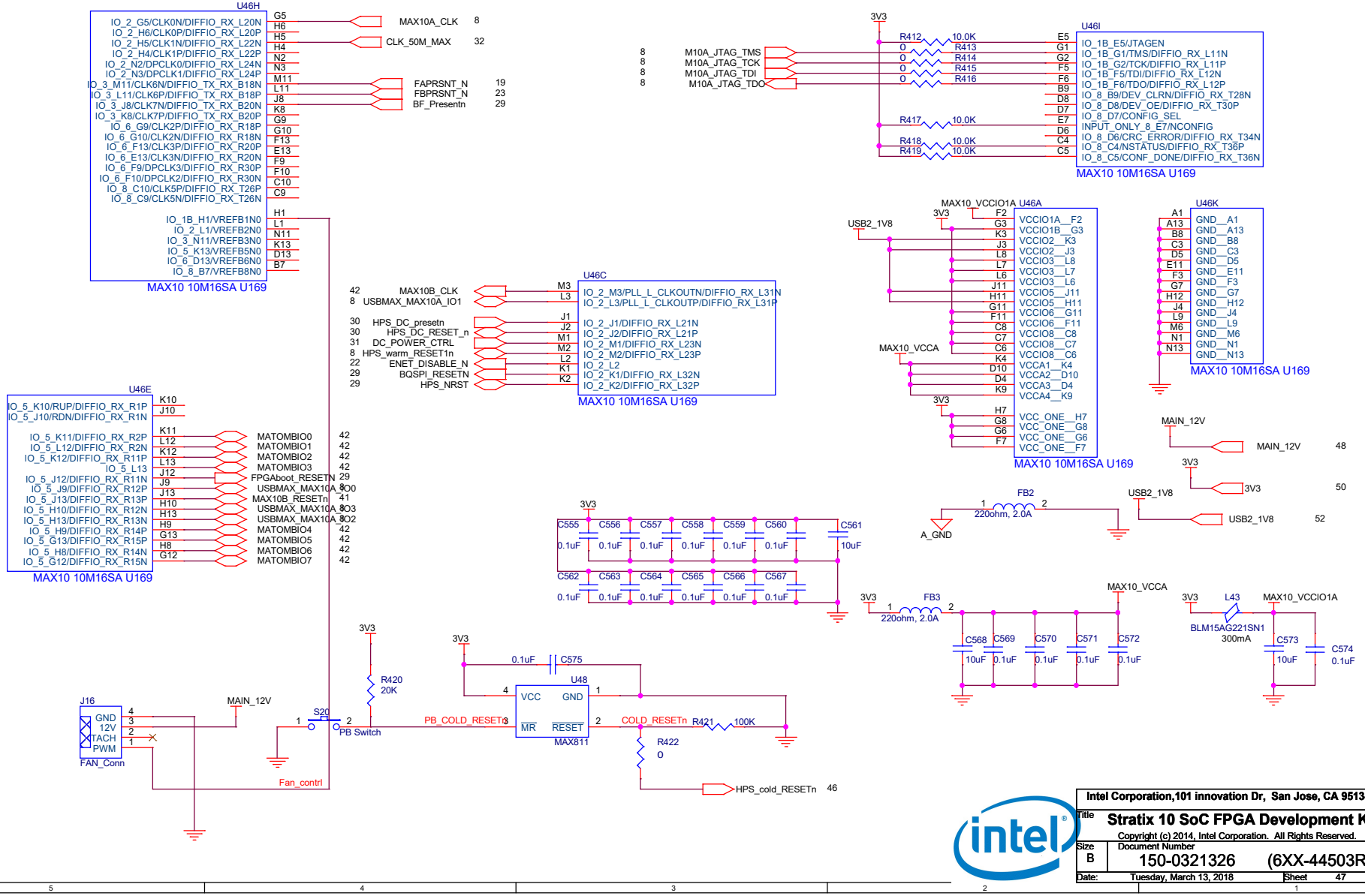
MAX10 PWR Manager 2



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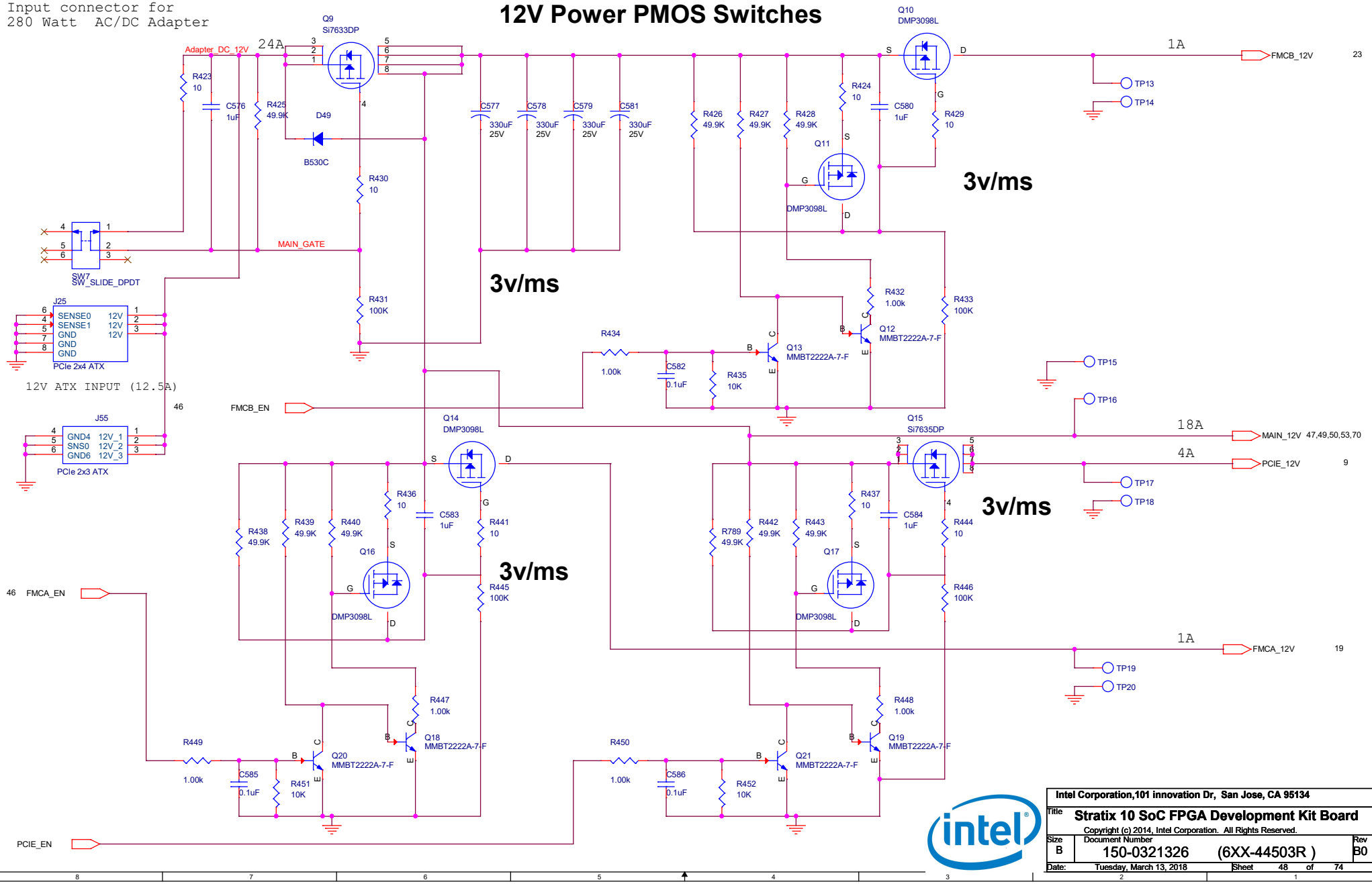
12V Power PMOS Switches

Input connector for
280 Watt AC/DC Adapter



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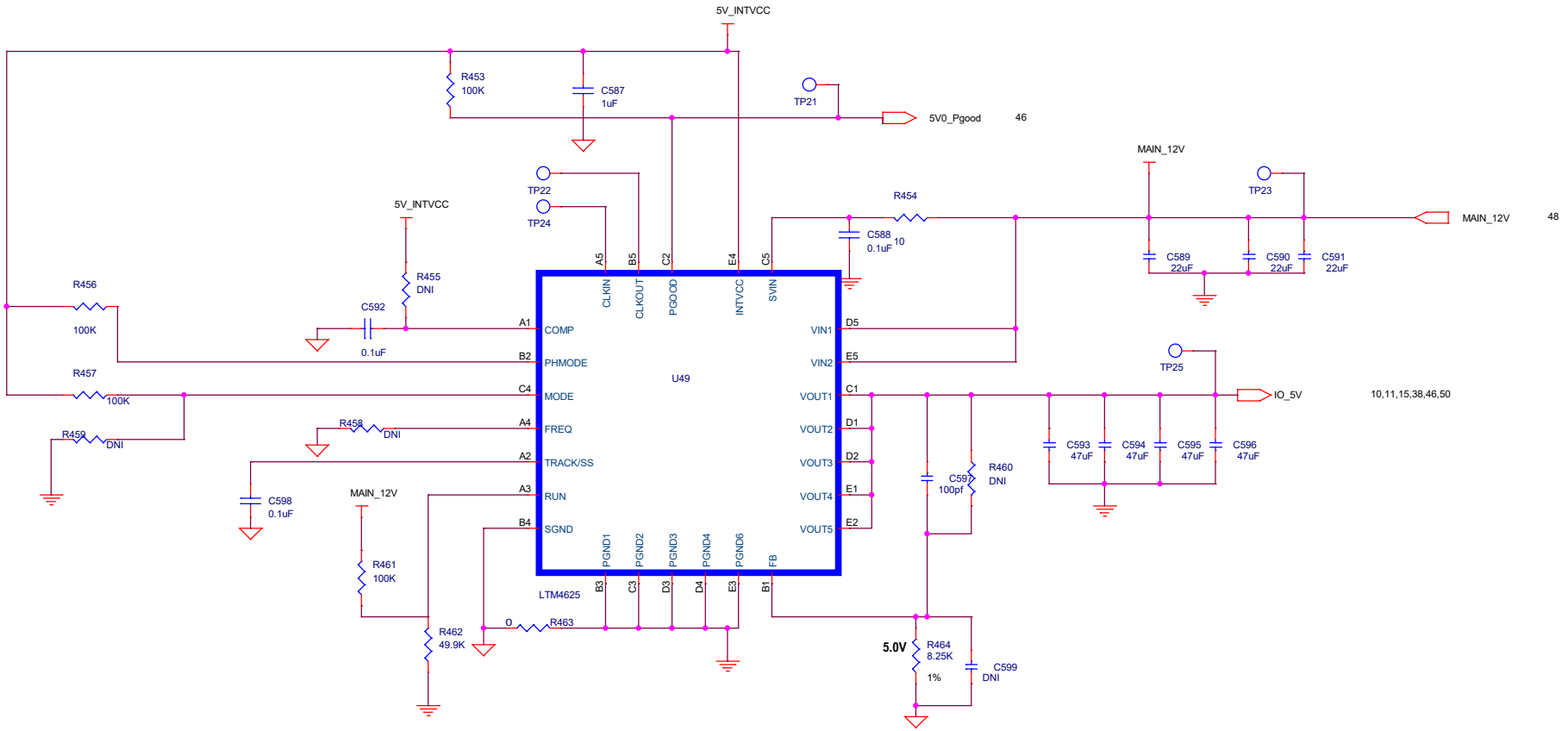
12V to 5V Power Supply



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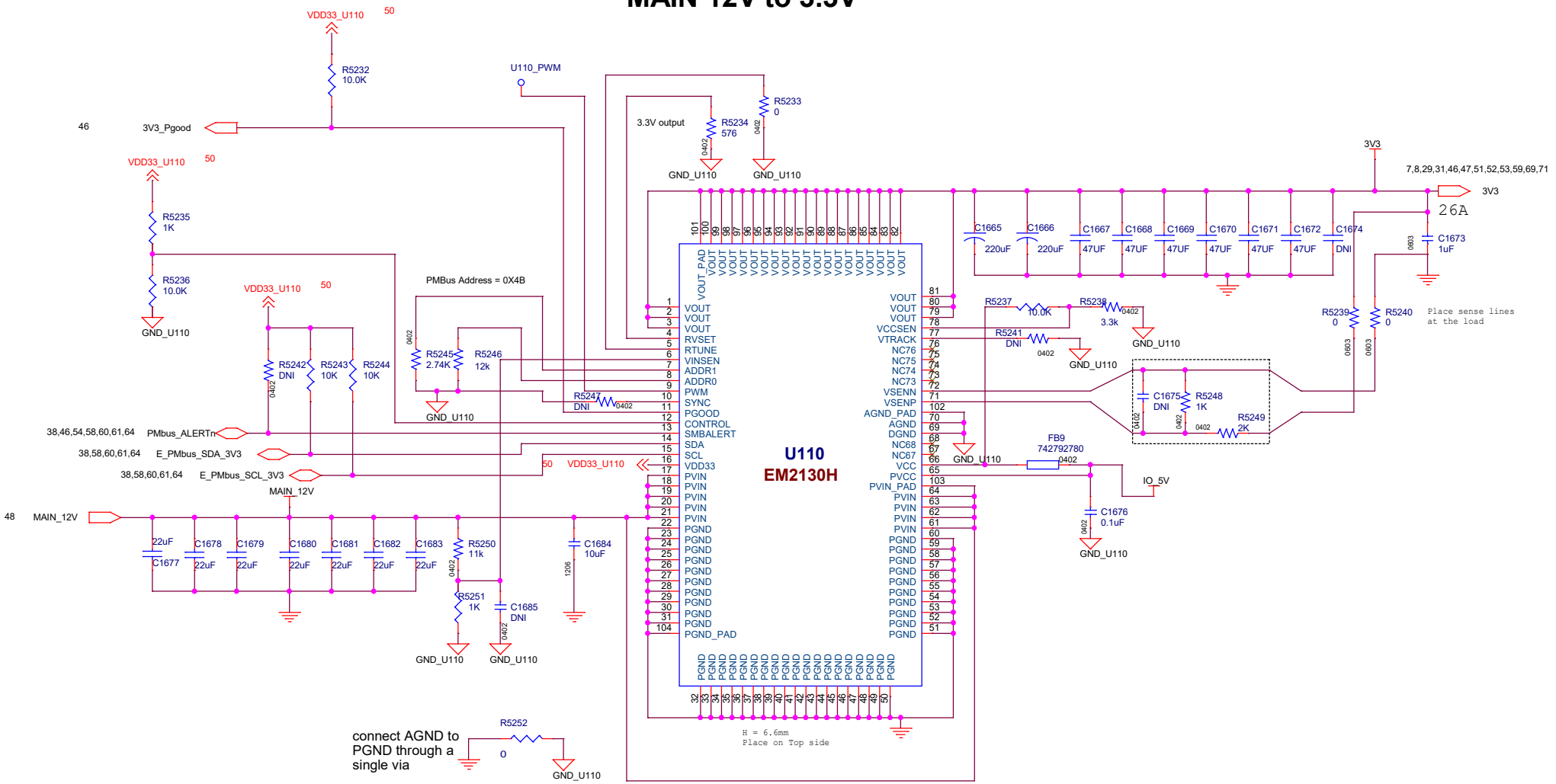
MAIN 12V to 3.3V



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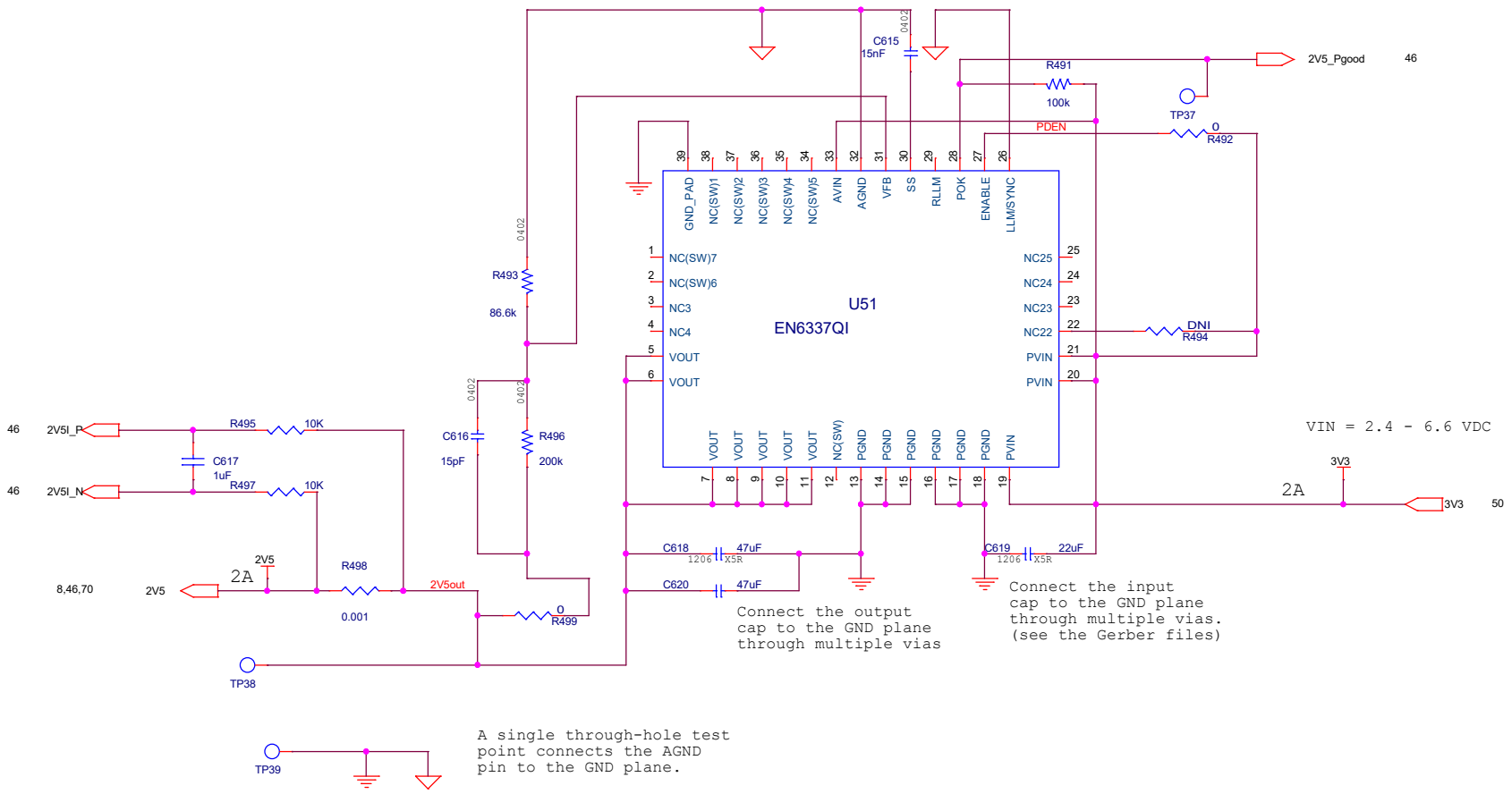
3V3 to 2V5 Converter



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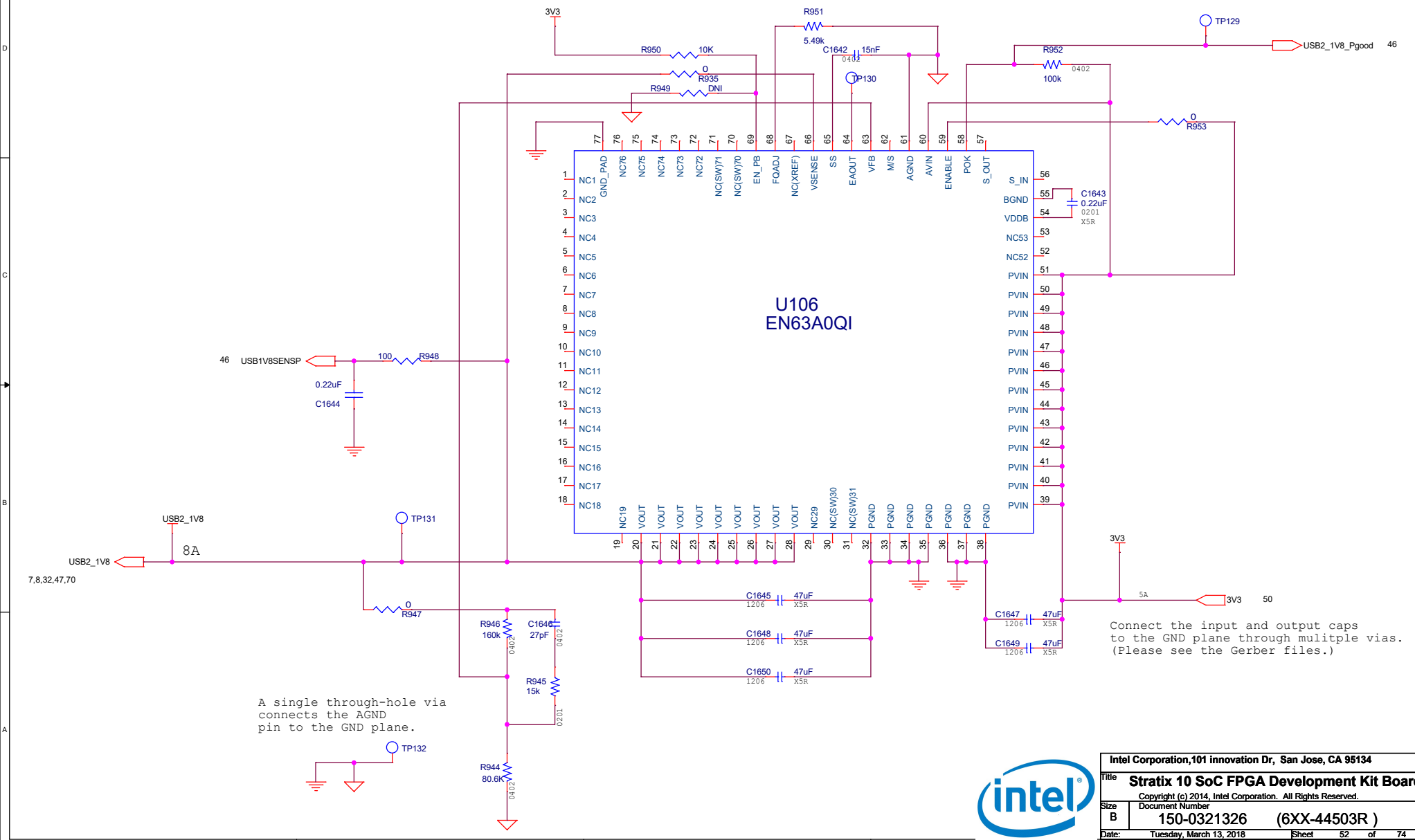
3.3V to 1.8V Converter



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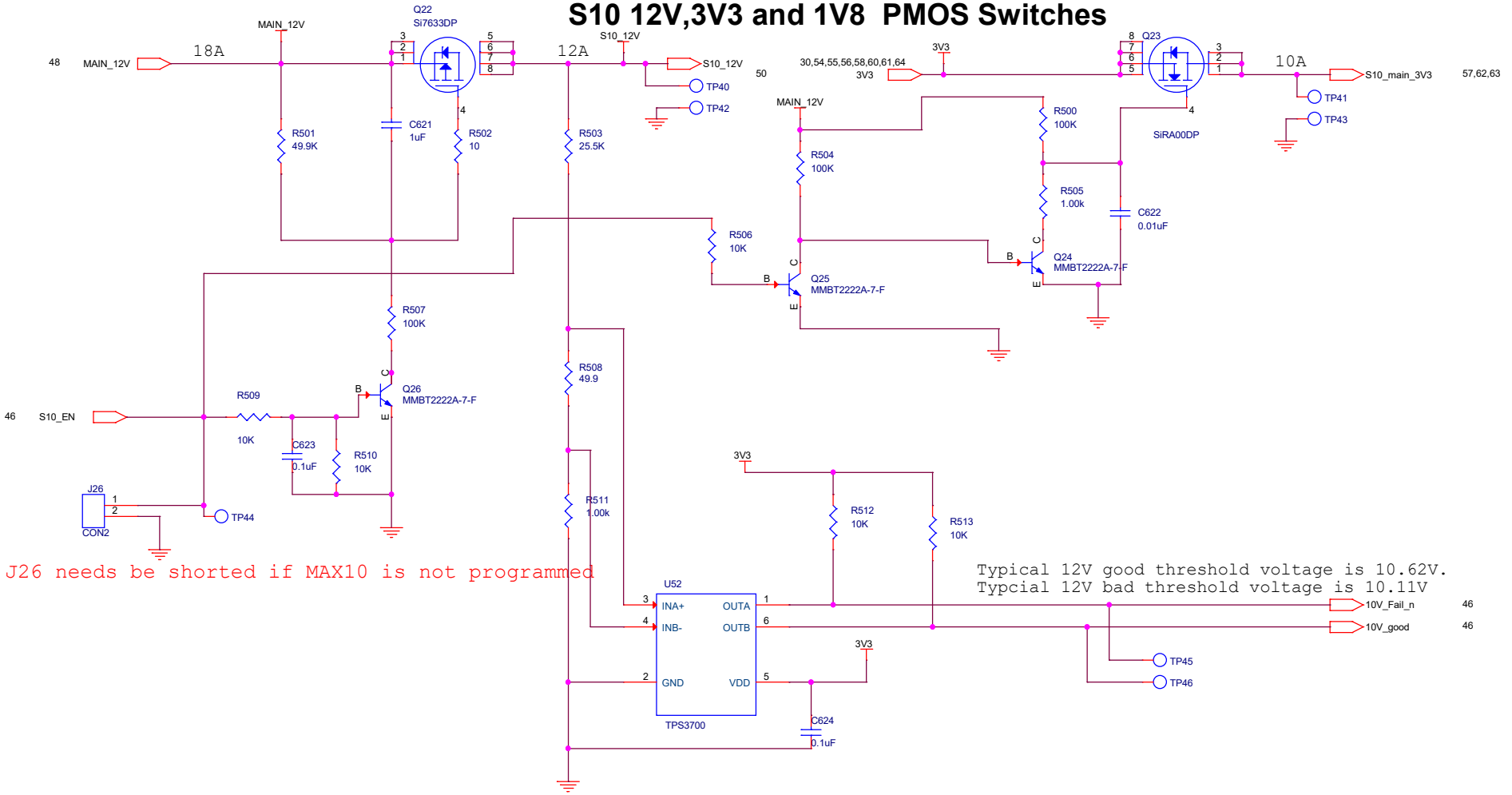
S10 12V,3V3 and 1V8 PMOS Switches



J26 needs be shorted if MAX10 is not programmed

Typical 12V good threshold voltage is 10.62V.
Typcial 12V bad threshold voltage is 10.11V

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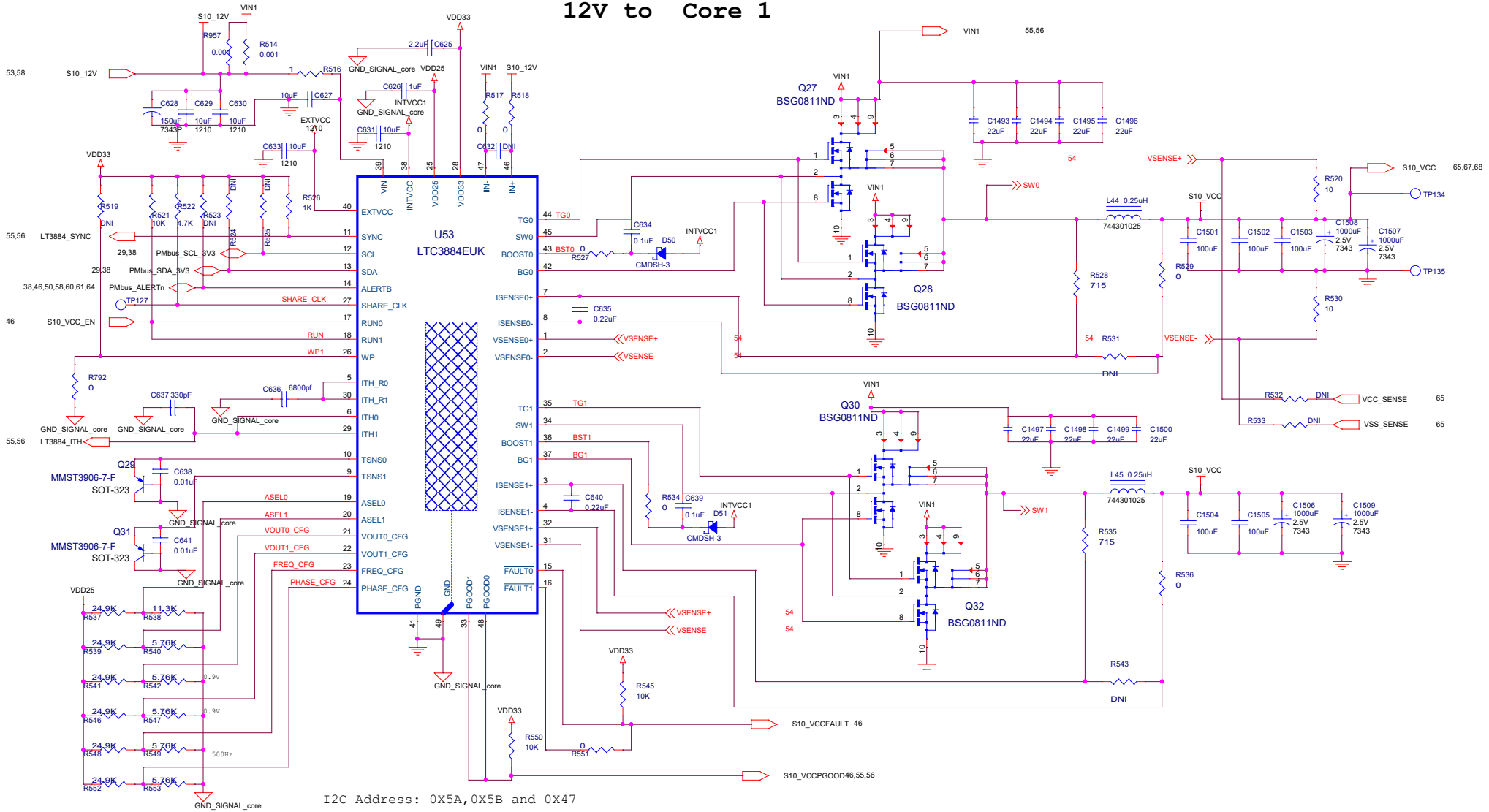
12V to Core 1



I2C Address: 0X5A,0X5B and 0X47

Check Phase define

Need 0.85V core voltage

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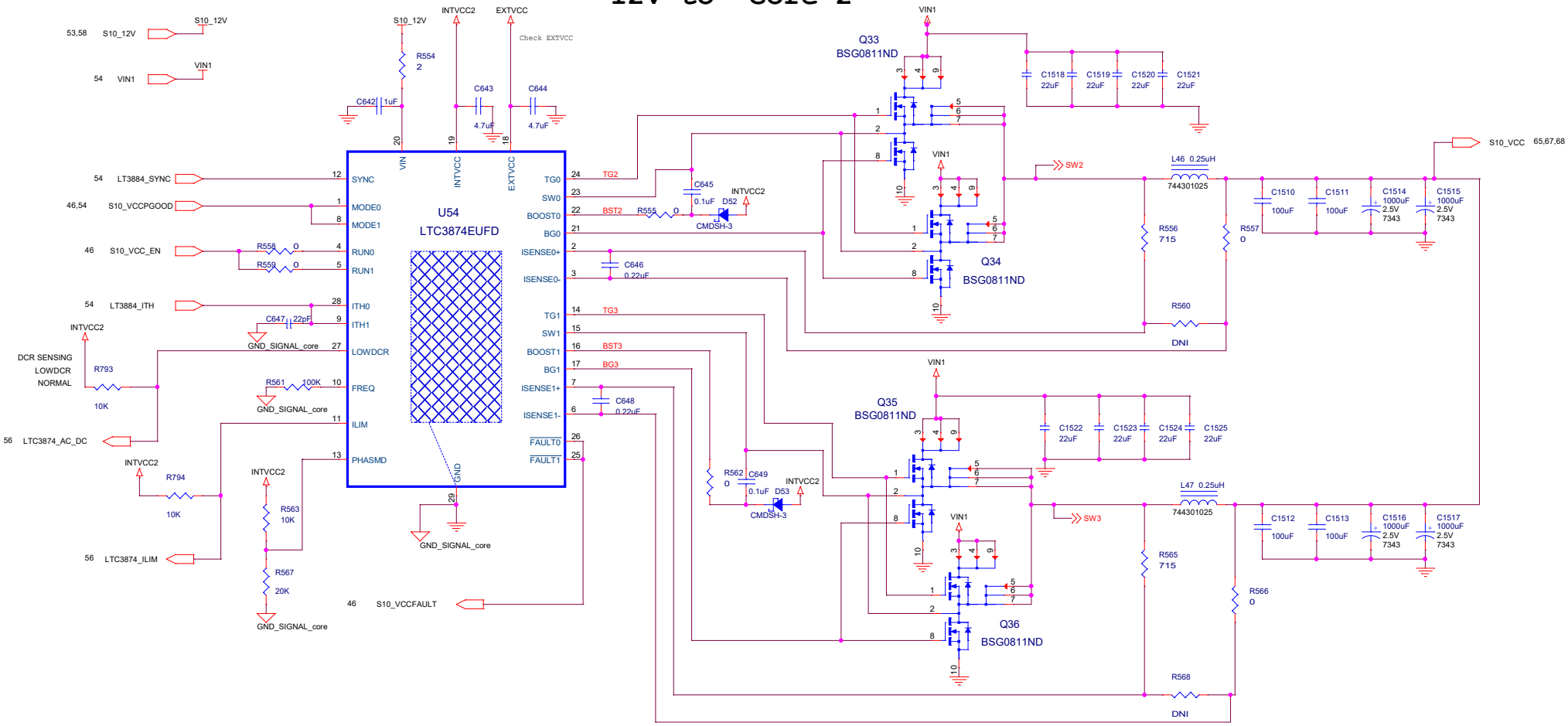
12V to Core 2



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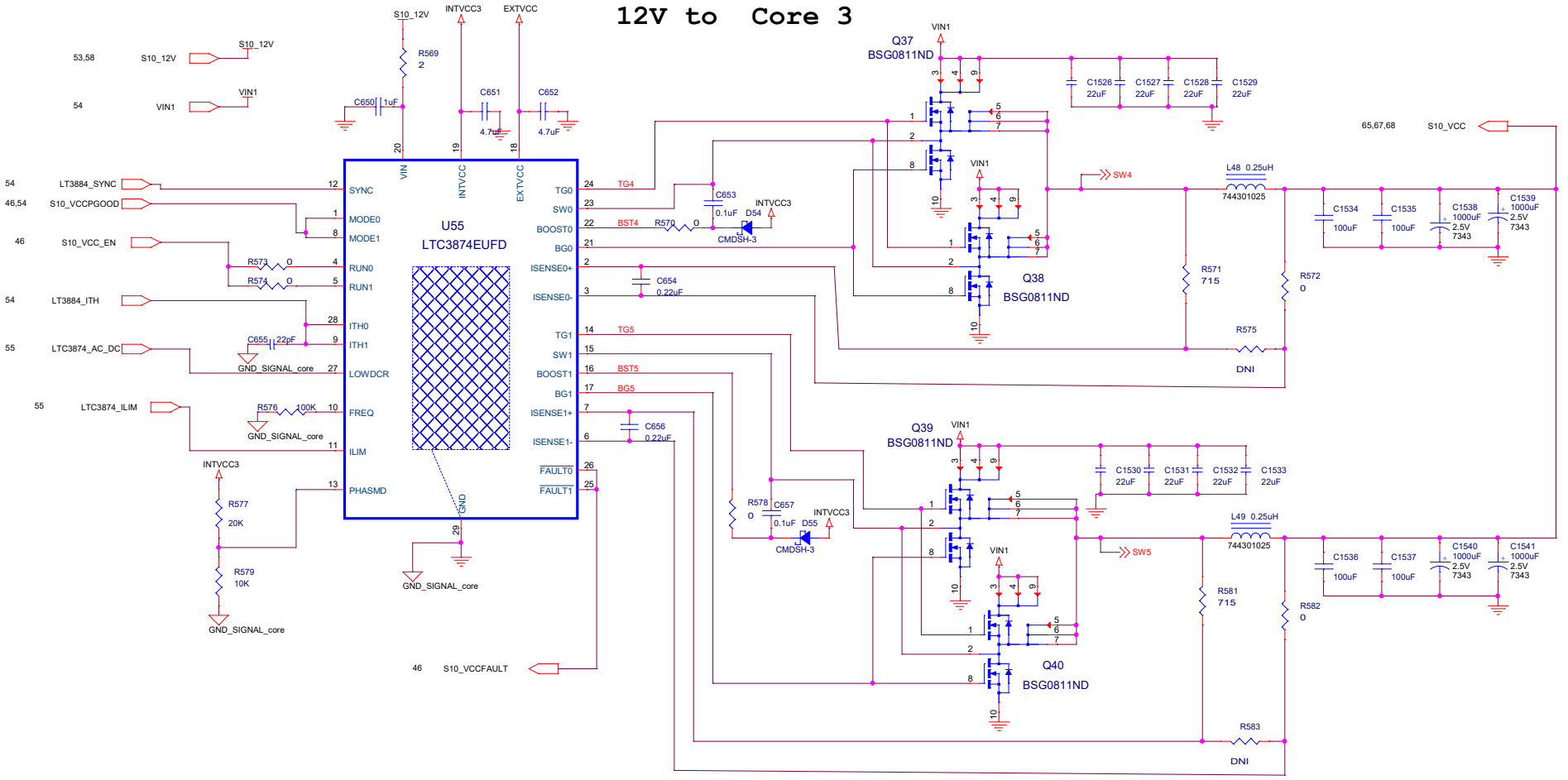
12V to Core 3



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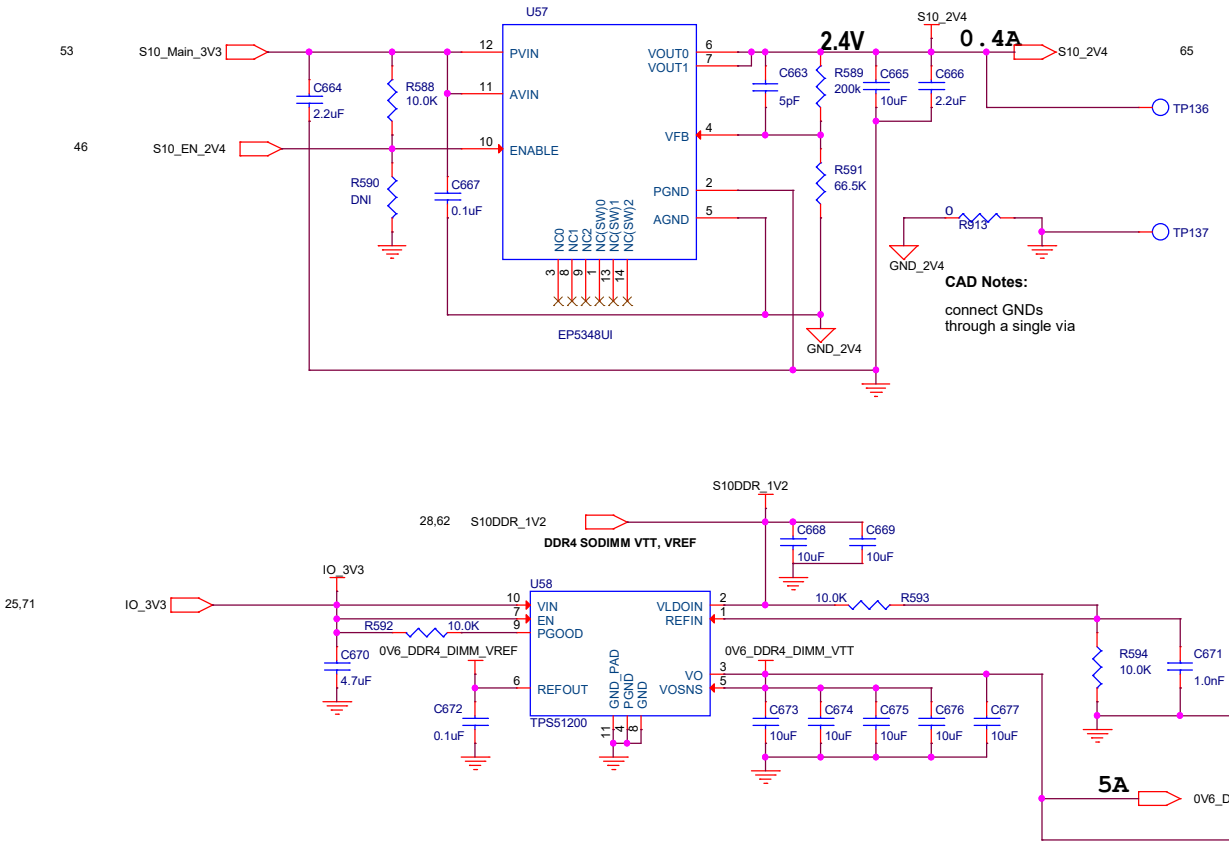
VTT & 2V4 Power



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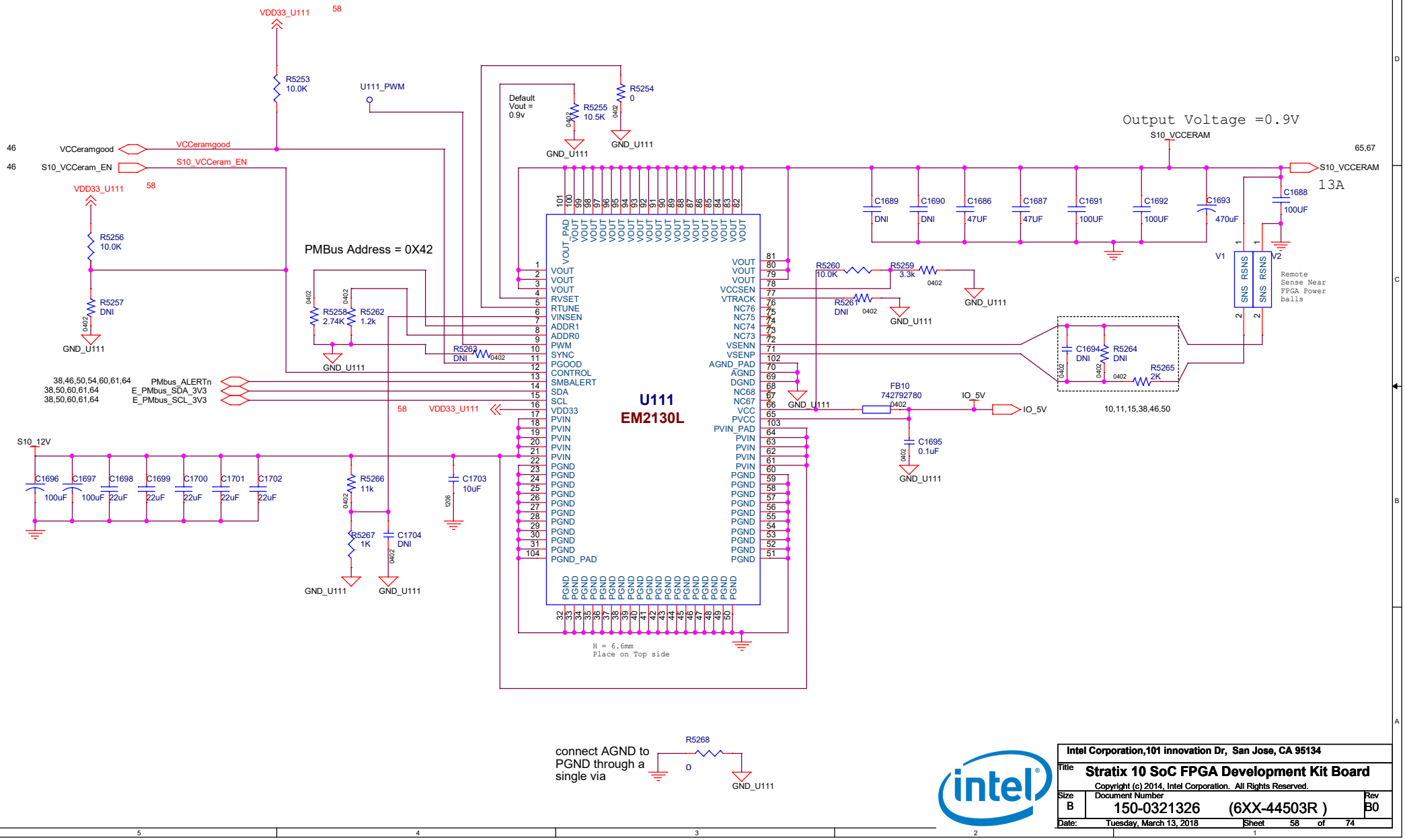
Power - S10 VCCERAM



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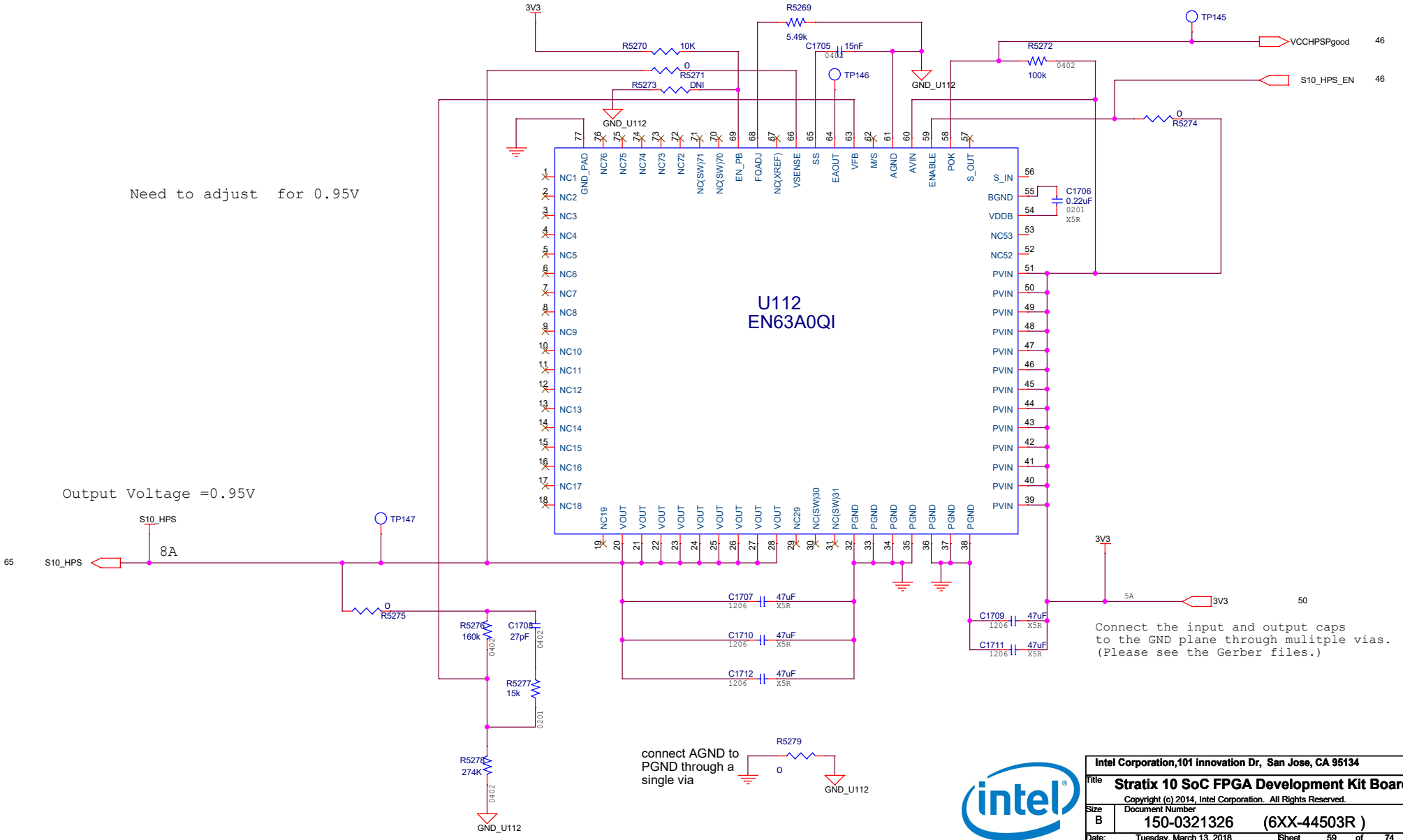
S10_HPS Supply



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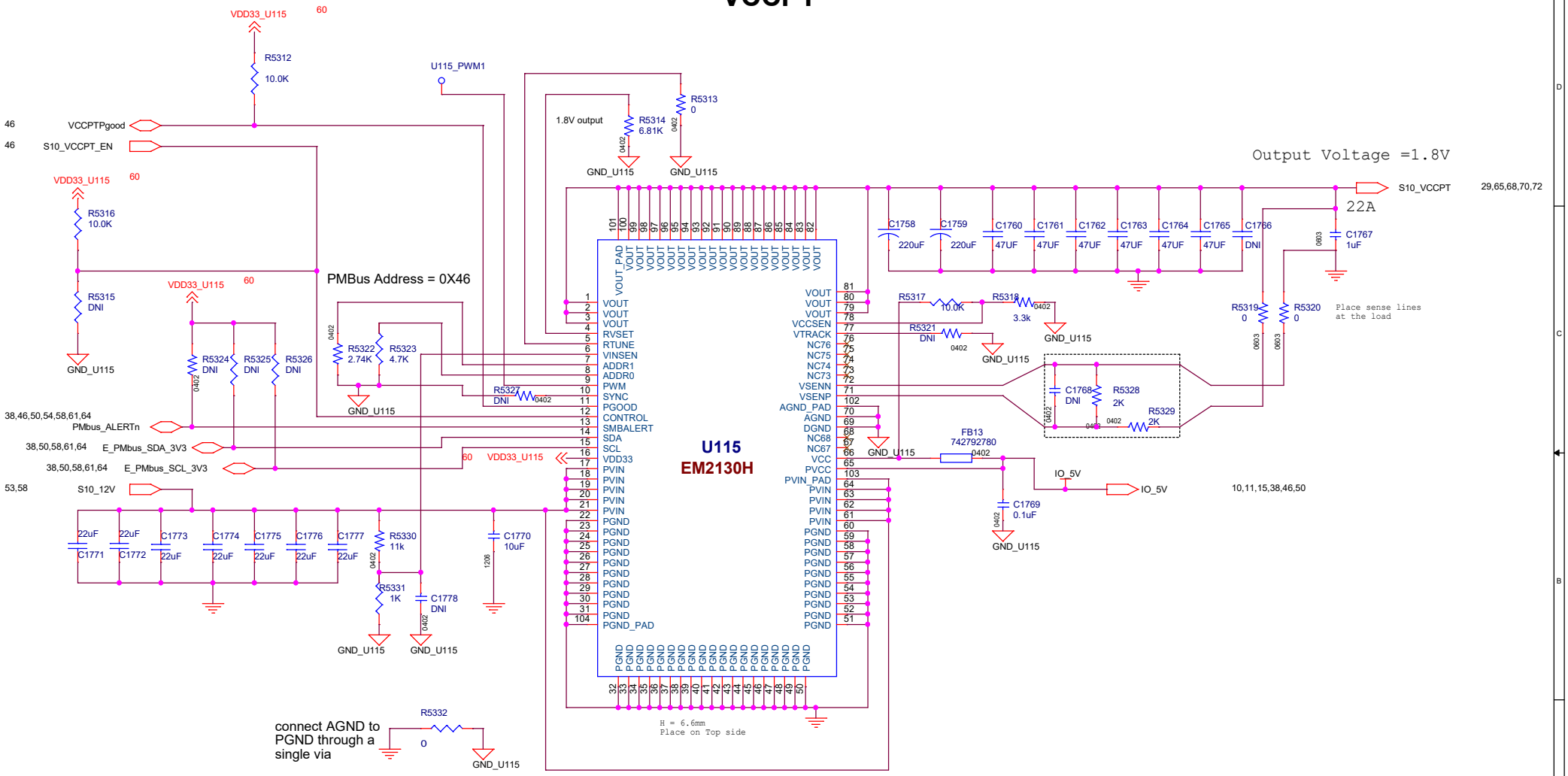
VCCPT



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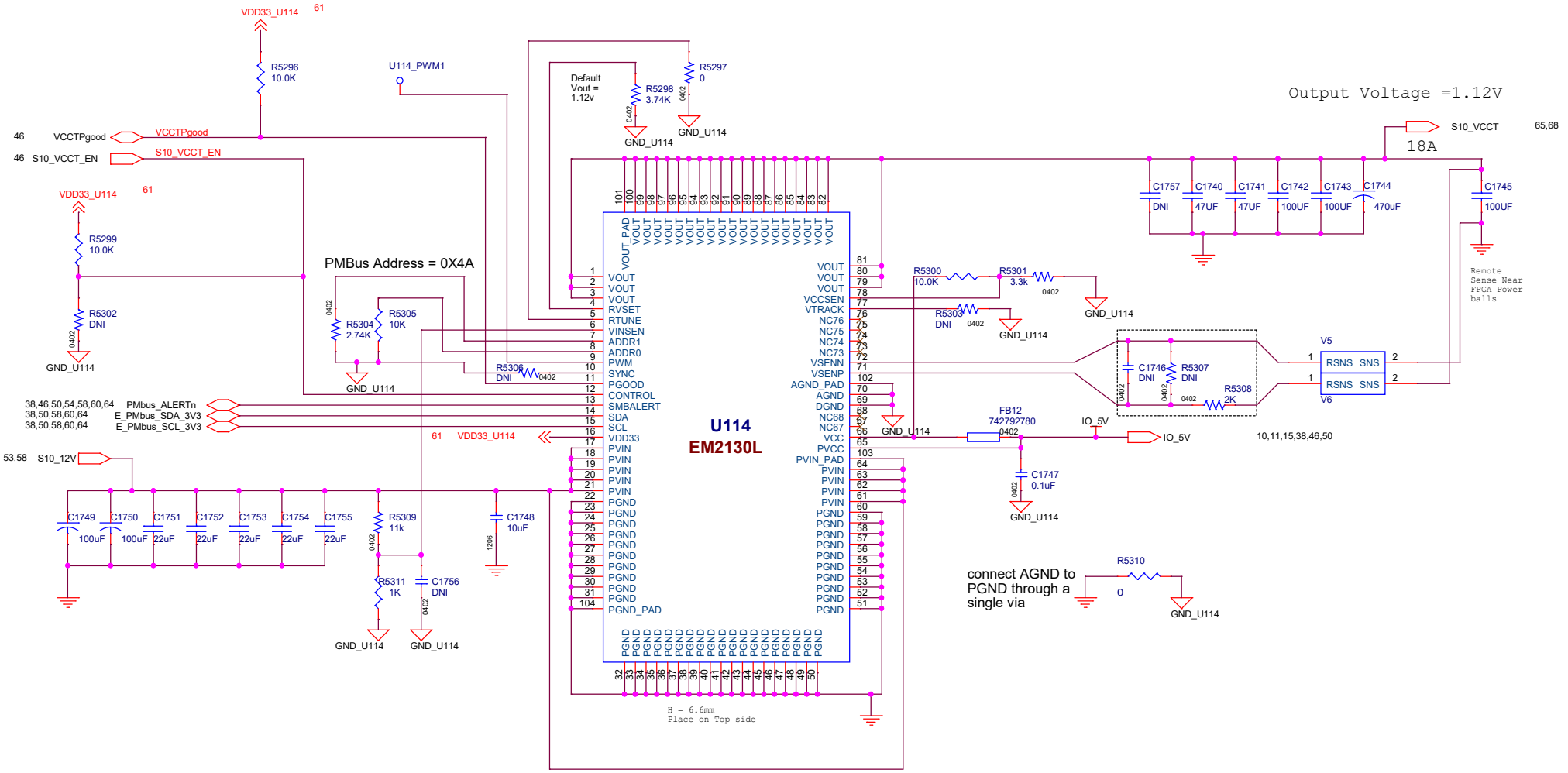
VCCT



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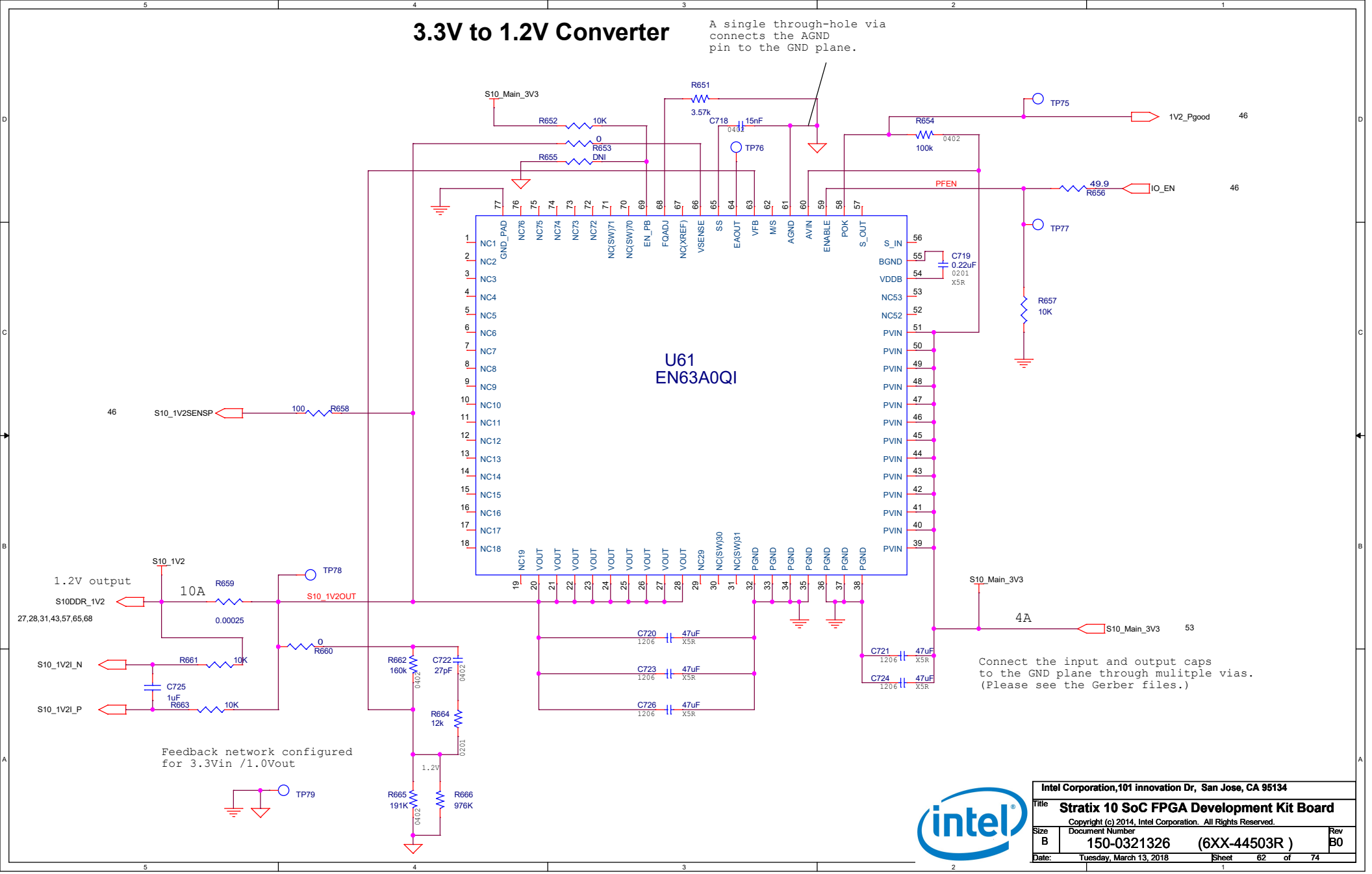
3.3V to 1.2V Converter



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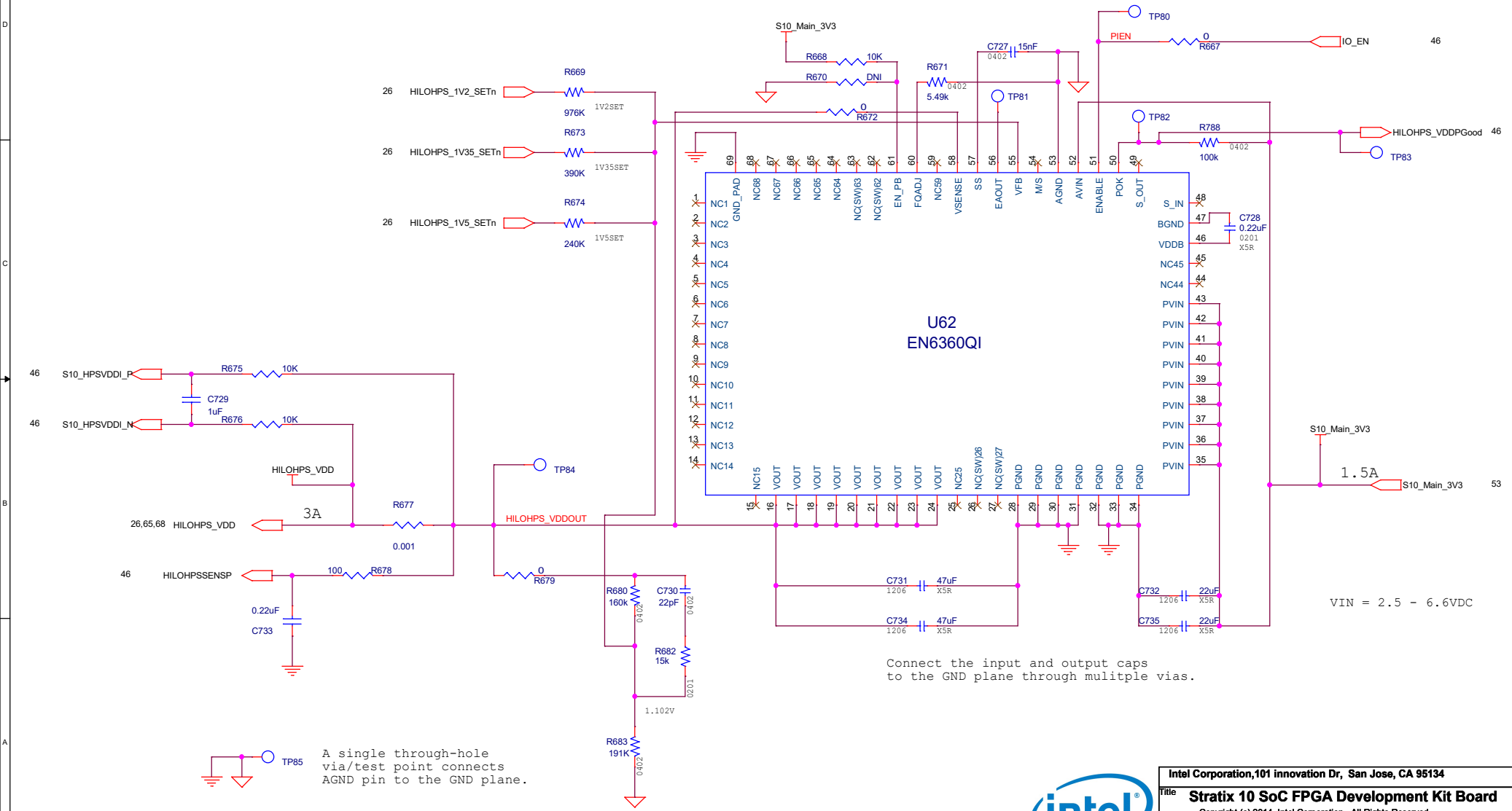
3.3V to HPS HILO VDD converter



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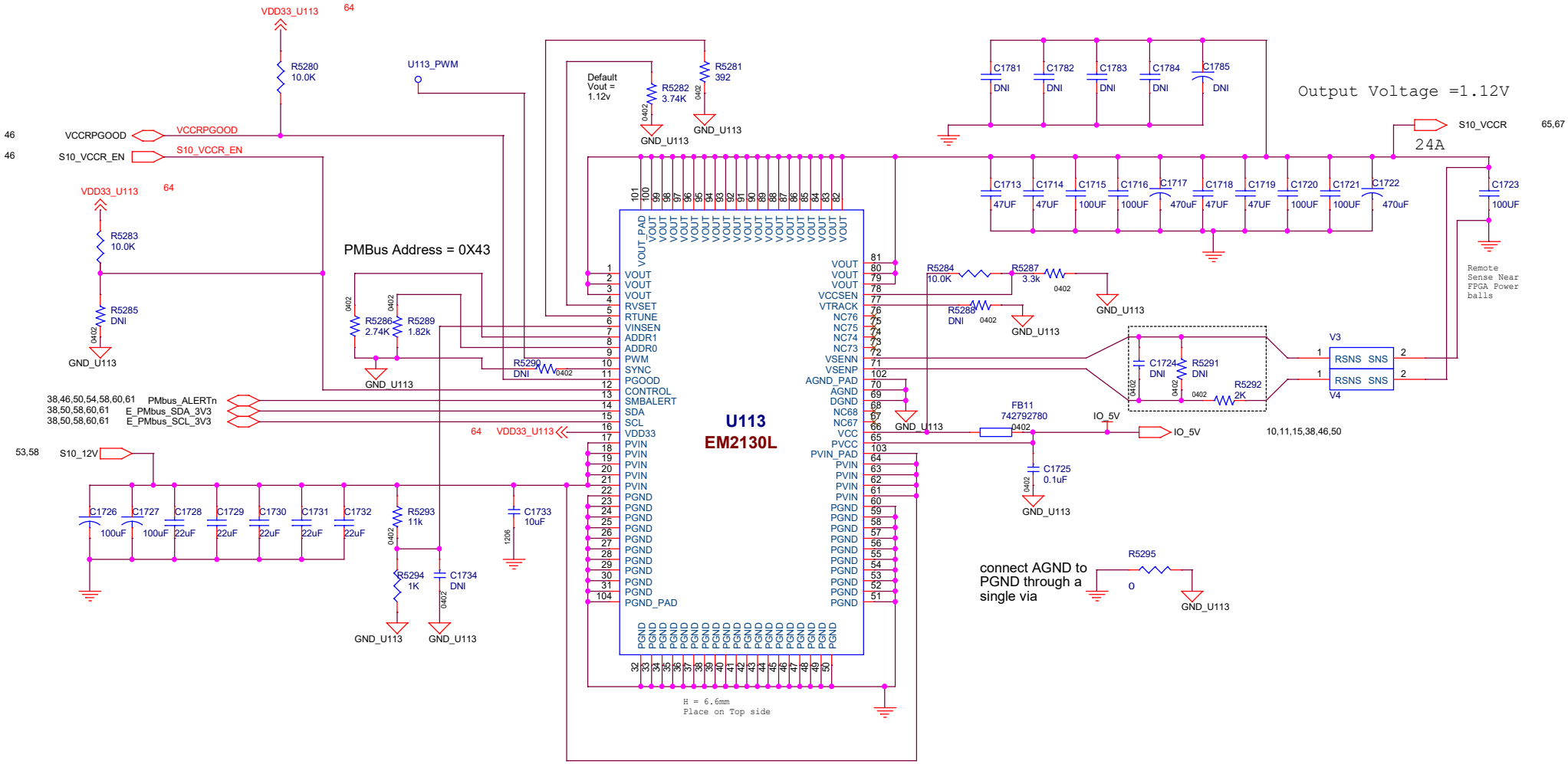
VCCR



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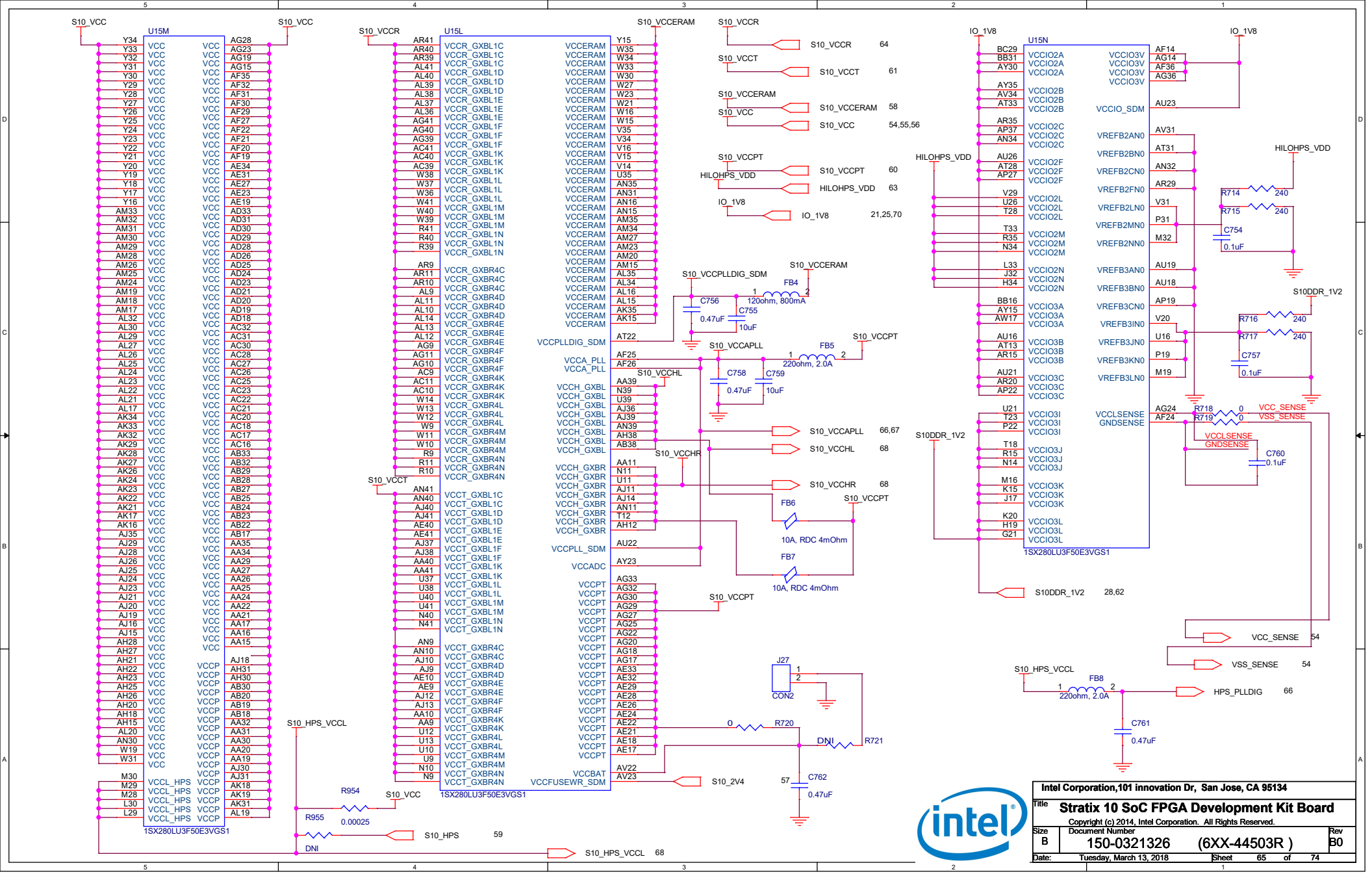
U15M
1SX280LU3F50E3VGS1
U15L
1SX280LU3F50E3VGS1
U15N
1SX280LU3F50E3VGS1
S10_VCC
S10_VCCR
S10_VCCERAM
S10_VCCT
S10_VCCPT
S10_VCCPLLDIG_SDM
S10_VCCAPLL
S10_VCCHL
S10_VCCHR
S10_HPS_VCCL
S10_HPS
S10_2V4
S10DDR_1V2
IO_1V8
HILOHPS_VDD
VCC_SENSE
VSS_SENSE
VCCLSENSE
GNDSENSE
HPS_PLLDIG
R954
0.00025
R955
DNI
R720
R721
C761
0.47uF
C762
0.47uF
J27
CON2
FB4
120ohm, 800mA
FB5
220ohm, 2.0A
FB6
10A, RDC 4mOhm
FB7
10A, RDC 4mOhm
FB8
220ohm, 2.0A
C756
0.47uF
C755
10uF
C758
0.47uF
C759
10uF
C760
0.1uF
C754
0.1uF
C757
0.1uF
R714
240
R715
240
R716
240
R717
240
R718
0
R719
0
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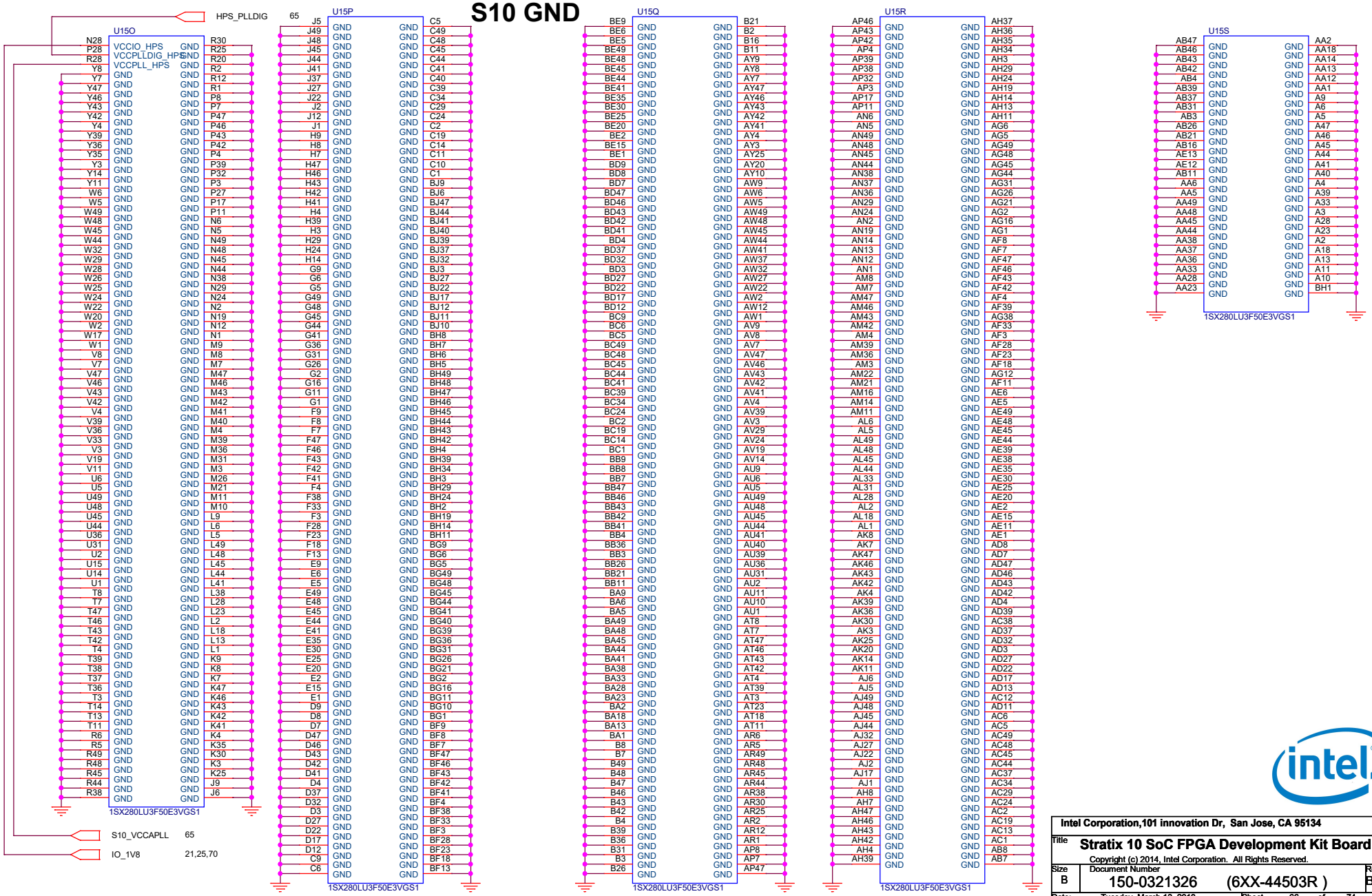
S10 GND



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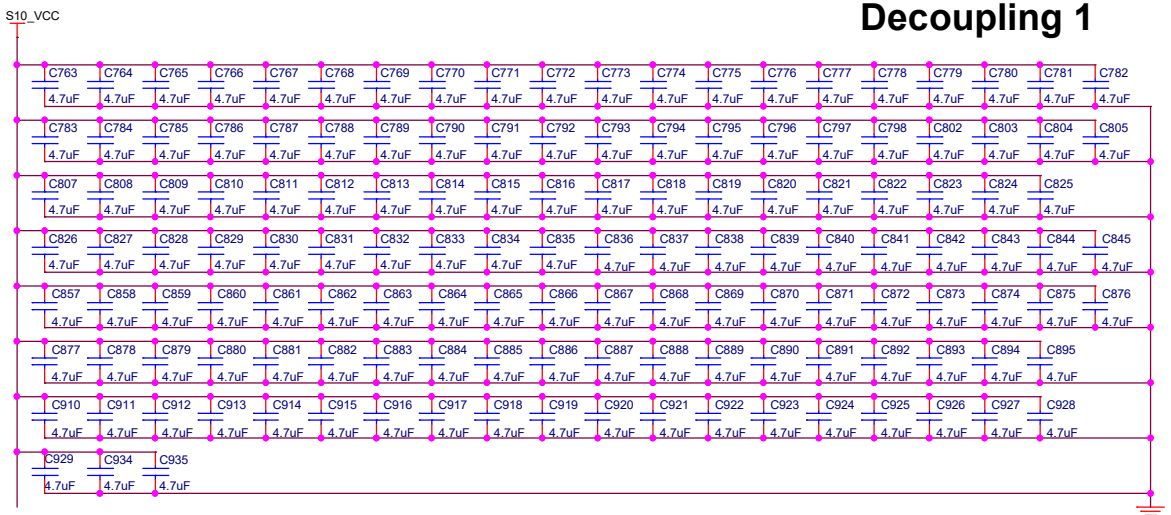
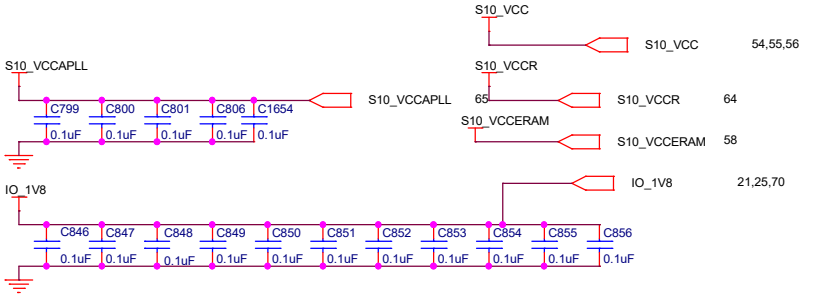
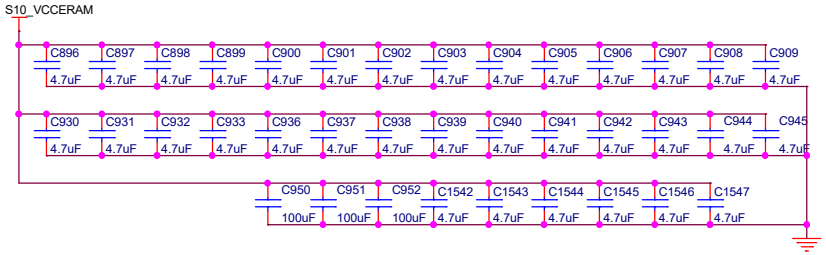
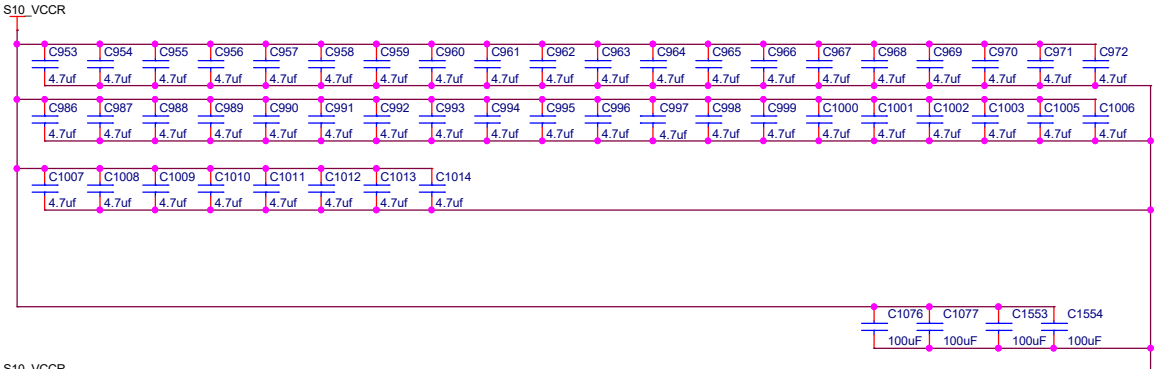
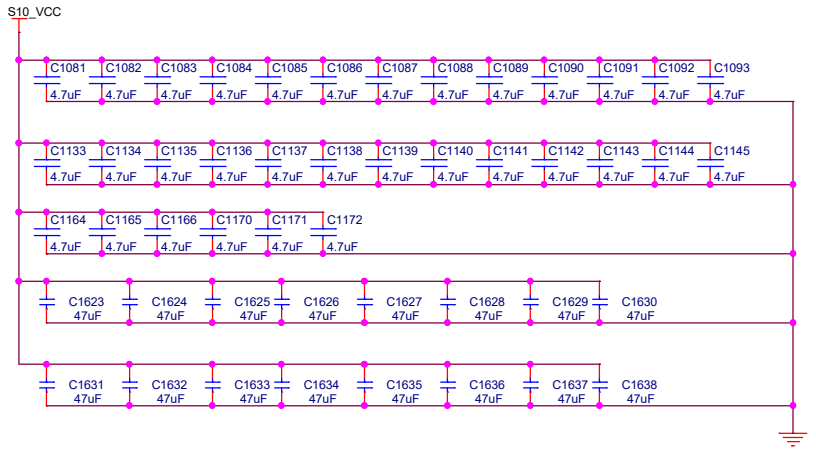
Decoupling 1

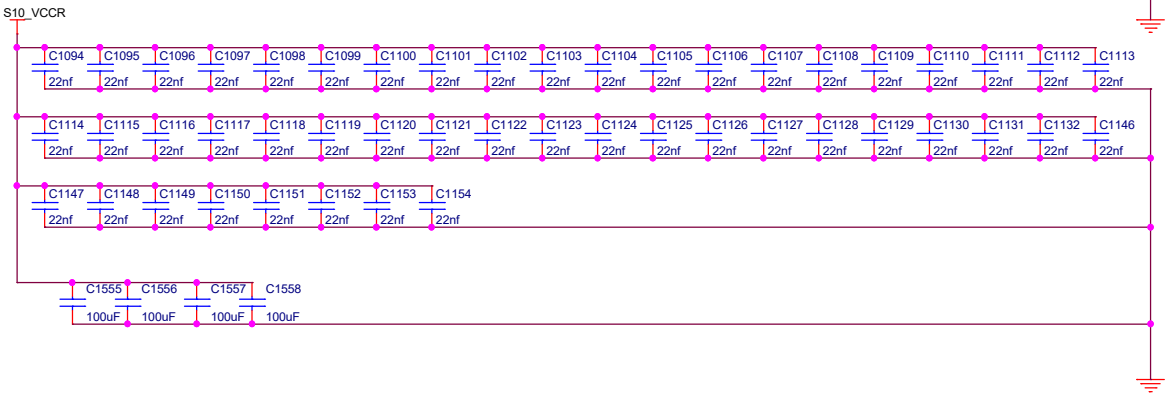












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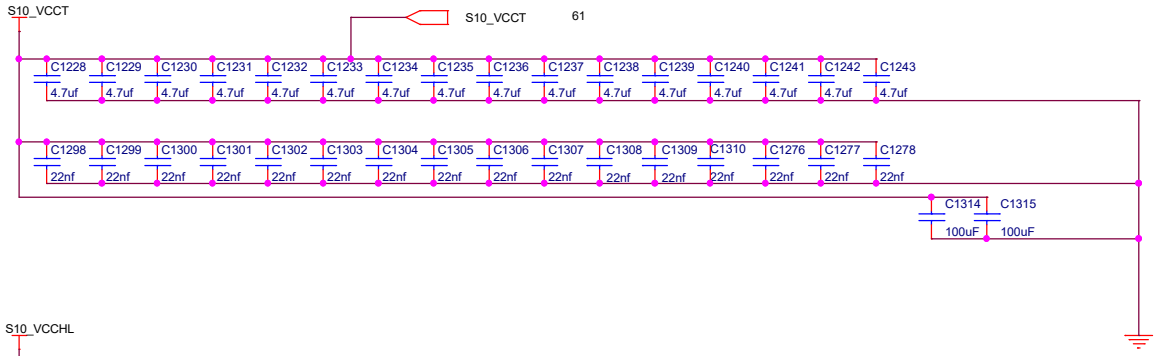
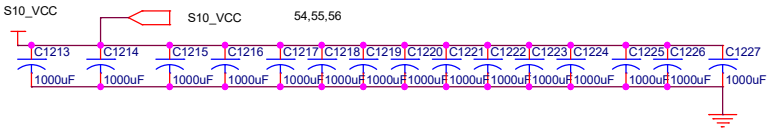
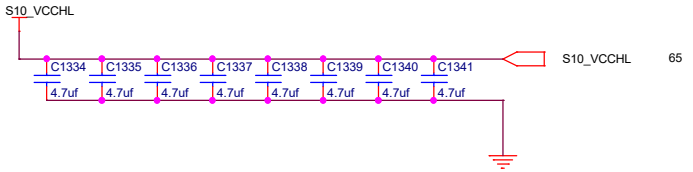
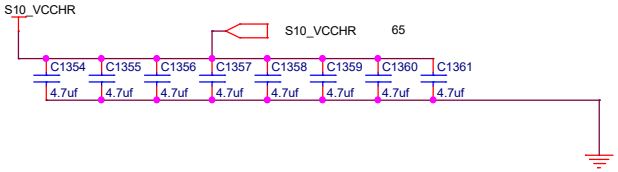
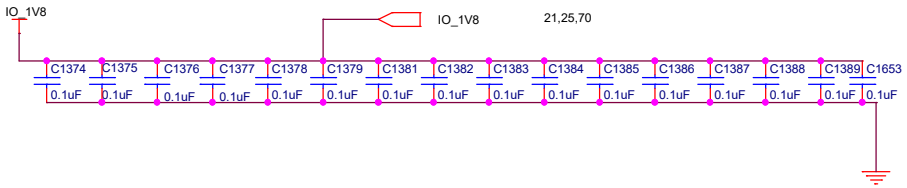
Decoupling 2

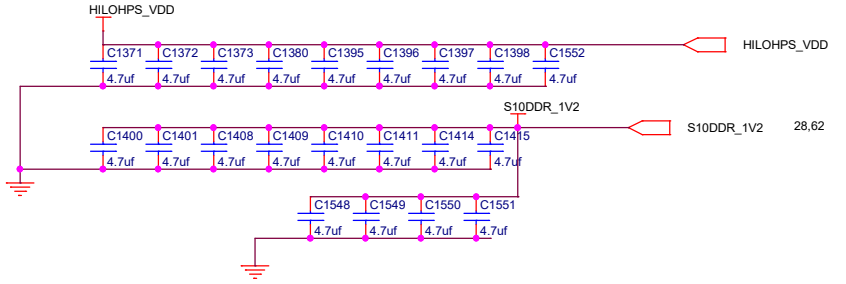


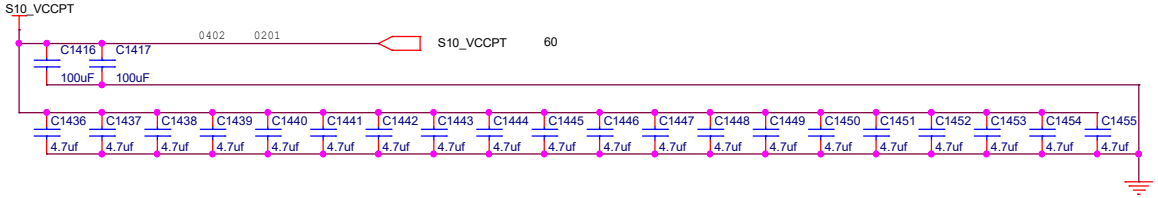


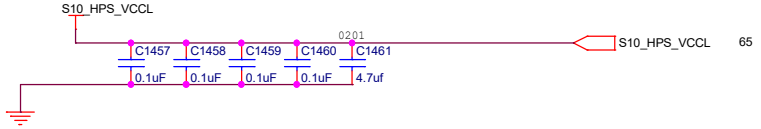












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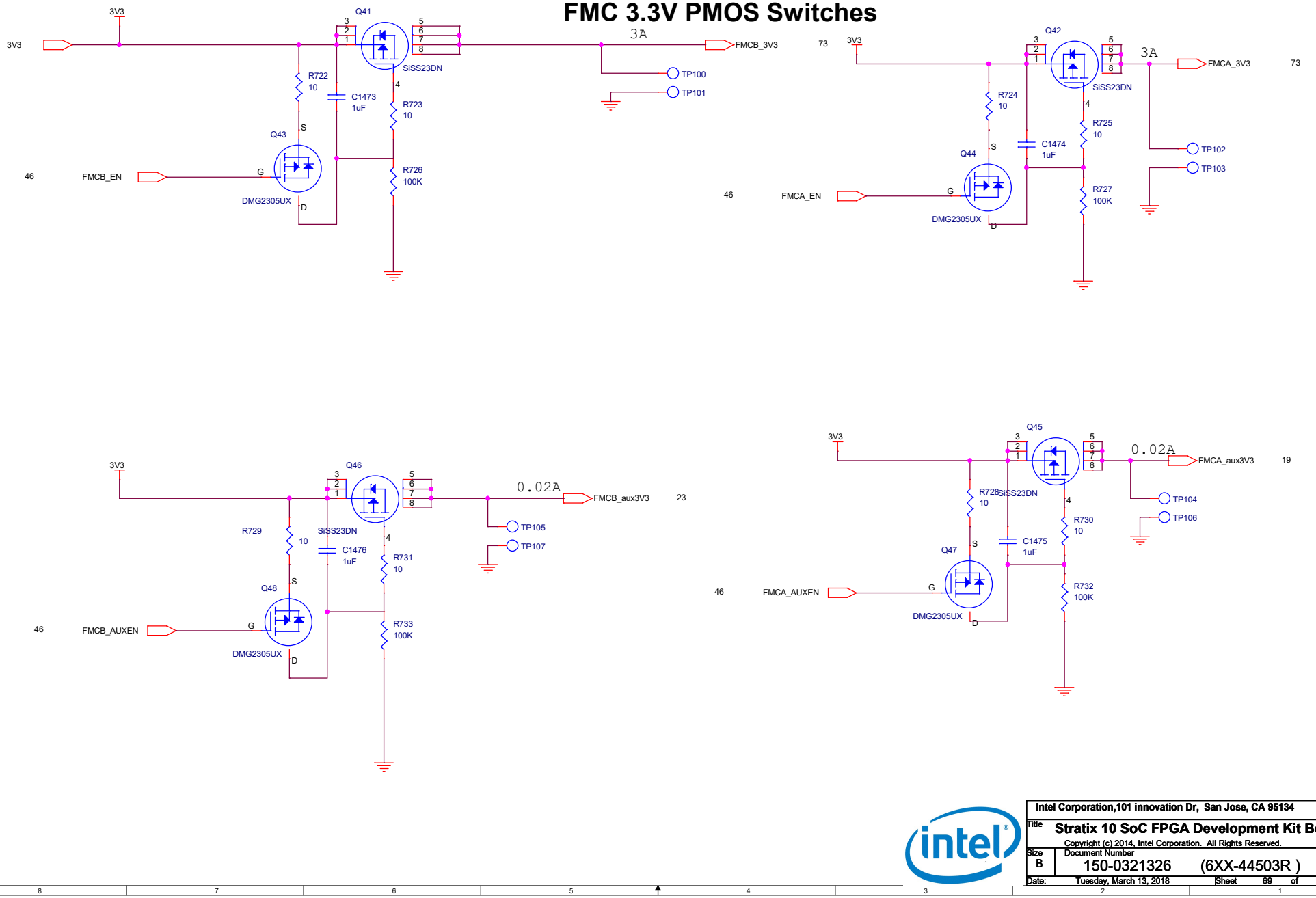
FMC 3.3V PMOS Switches



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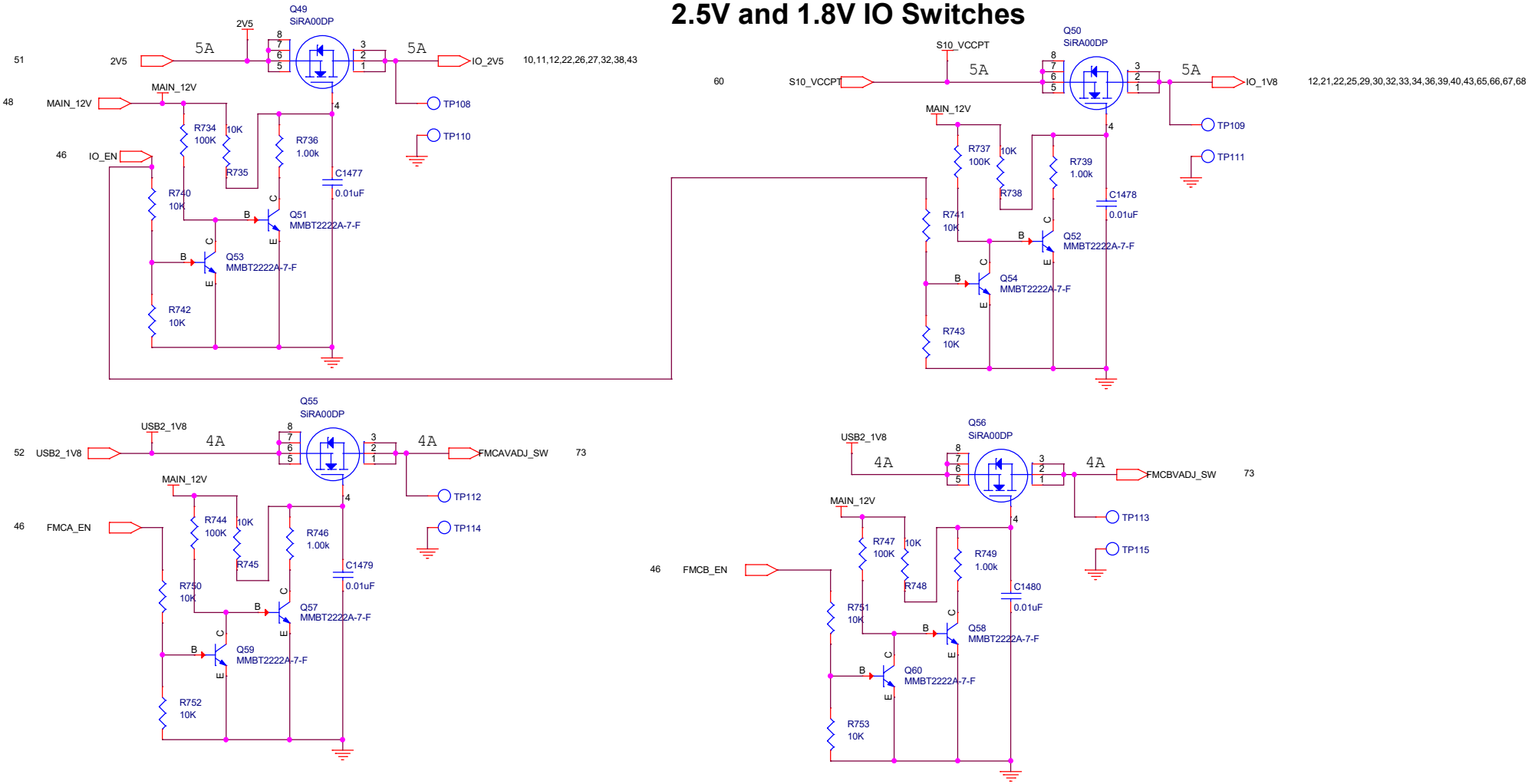
2.5V and 1.8V IO Switches



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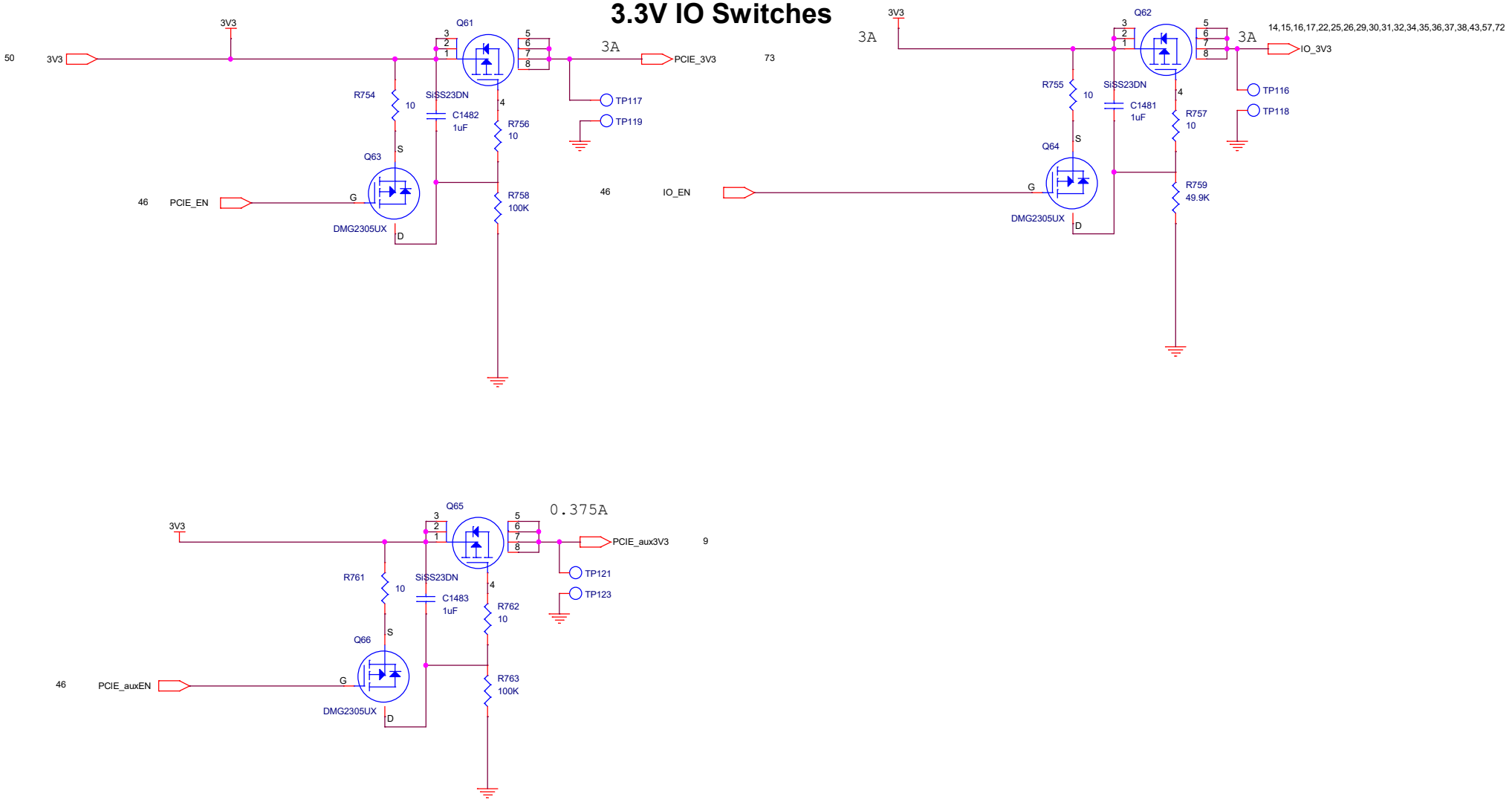
3.3V IO Switches



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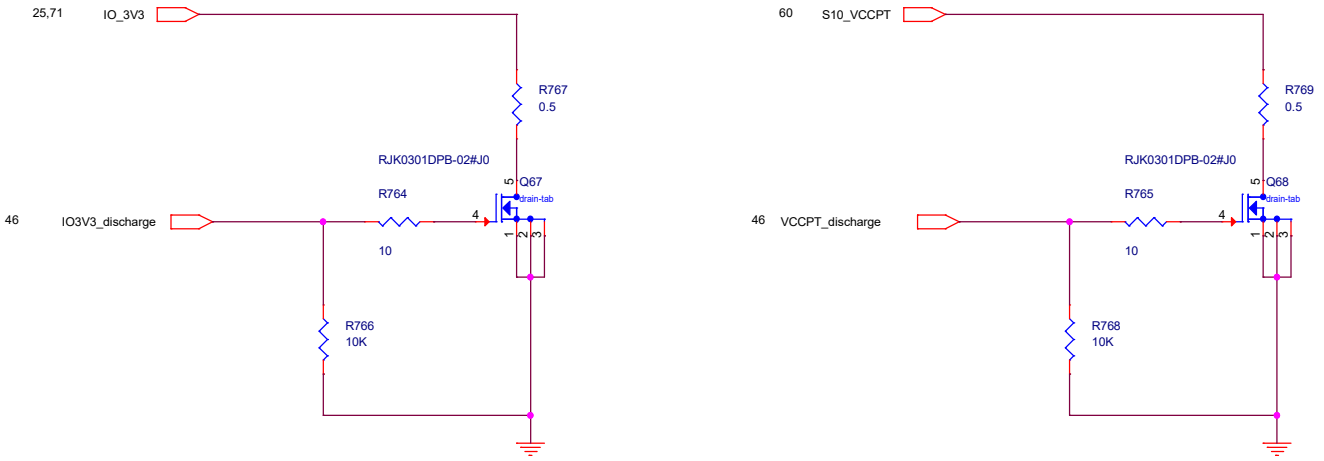
3.3V and 1.8V Discharge Load



50us Discharge time

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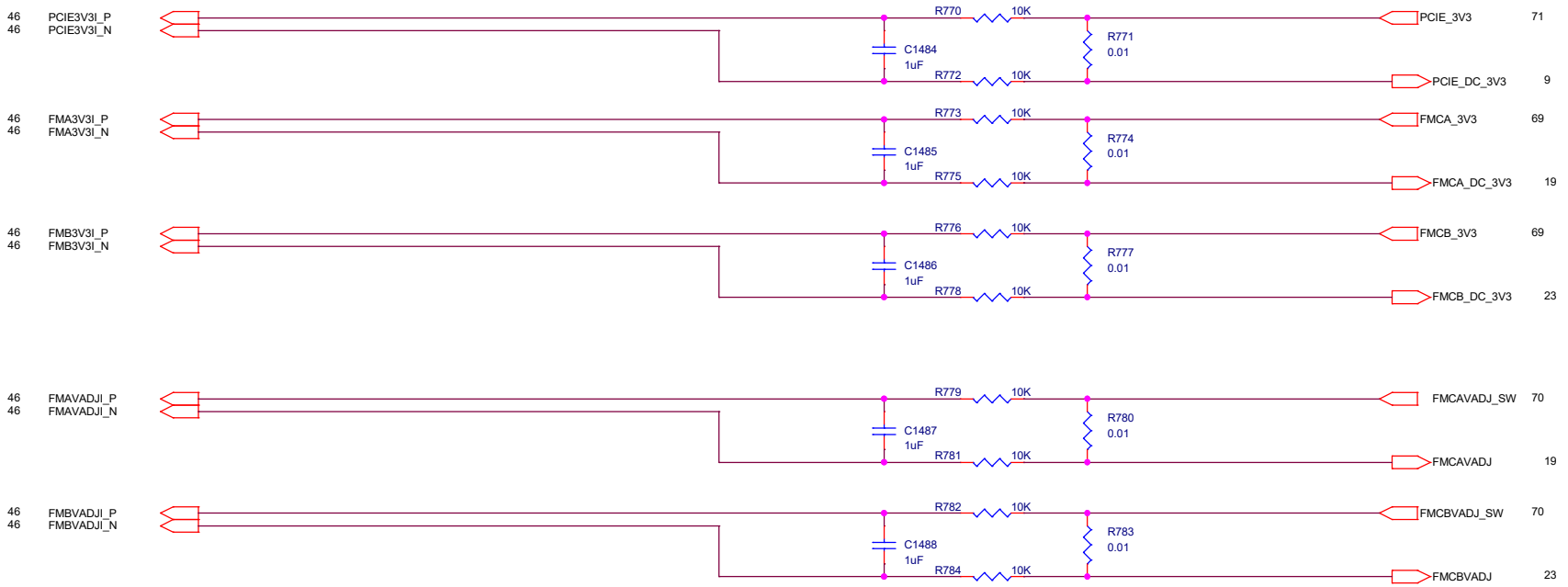
User DC card 3.3V Current Sensors



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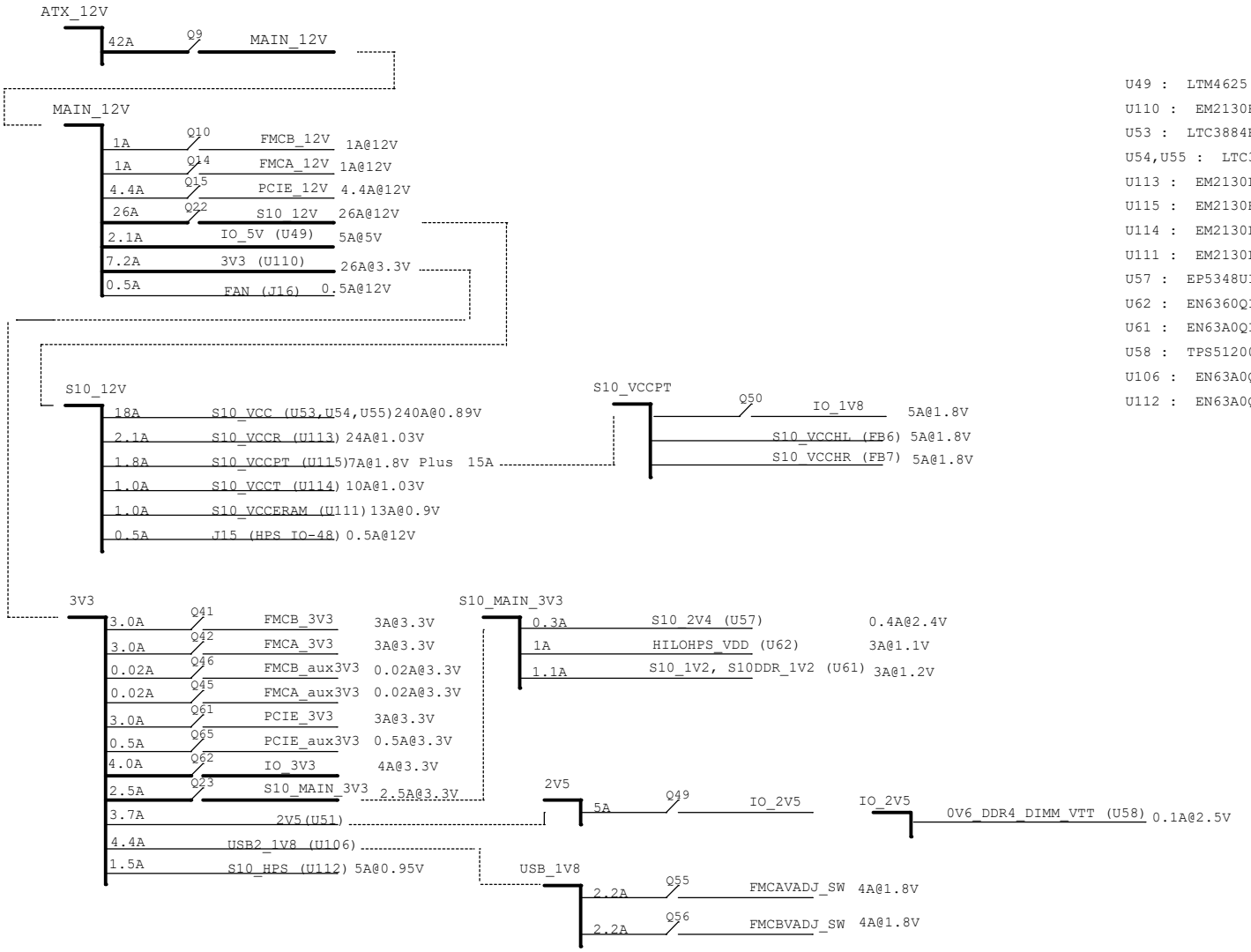
System Power Connection Chart



U49 : LTM4625
U110 : EM2130H
U53 : LTC3884EUK
U54,U55 : LTC3874EUFD
U113 : EM2130L
U115 : EM2130H
U114 : EM2130L
U111 : EM2130L
U57 : EP5348UI
U62 : EN6360QI
U61 : EN63A0QI
U58 : TPS51200
U106 : EN63A0QI
U112 : EN63A0QI

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