Intel Corporation
101 Innovation Drive
San Jose, CA 95134

April 5, 2022

NGC
Attn: Richard Rameriz

Subject: Intel FPGA USB Download Cable (formerly the USB Blaster)

Dear Richard Rameriz,

This letter is intended to outline the memory sources within the Intel® FPGA USB Download programming cable [PL-USB-BLASTER-RCN] and their level of volatility. The Intel FPGA USB Download programming cable has four sources of memory:

(1) Configuration memory (Serial EEPROM)
    a. 128 bytes
(2) USB FIFO memory (RAM memory inside USB FIFO interface chip)
    a. 512 bytes
(3) CPLD logic device (volatile part)
    a. Up to 64 flip-flops
(4) CPLD logic device (non-volatile part)
    a. 3844 bytes

With one exception, user programs or operating systems cannot write data to this memory during normal operation. The exception is the USB FIFO memory. Although data can be written to the USB FIFO memory, the data is not retained when powered off. Furthermore, data can be purged from the USB FIFO memory by removing the power.

Should you have any additional questions or require more information, please do not hesitate to contact me.

Best Regards,

Alyanna Castillo
Platform Solutions Product Marketing
Intel Corporation