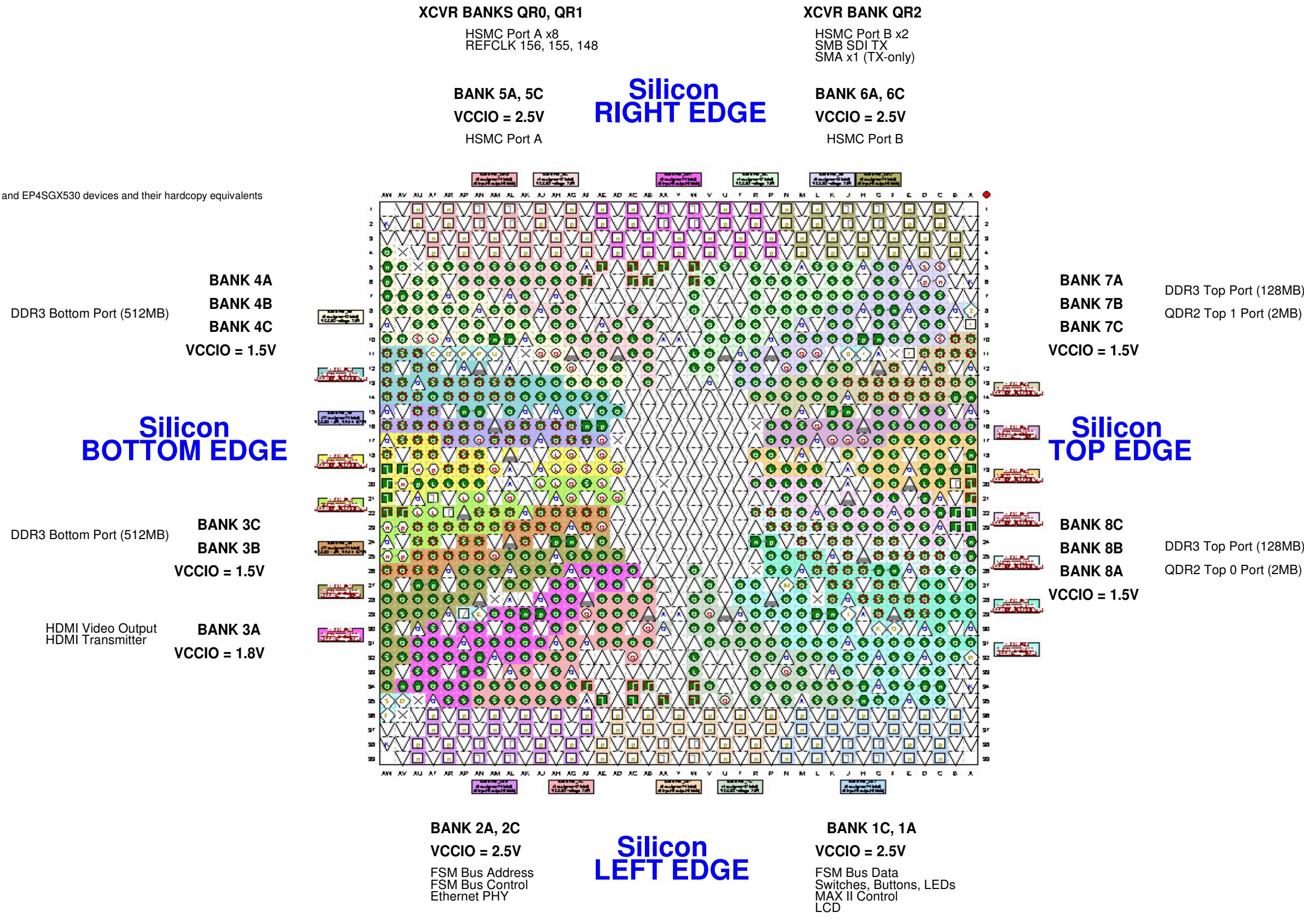


FPGA Package Top View

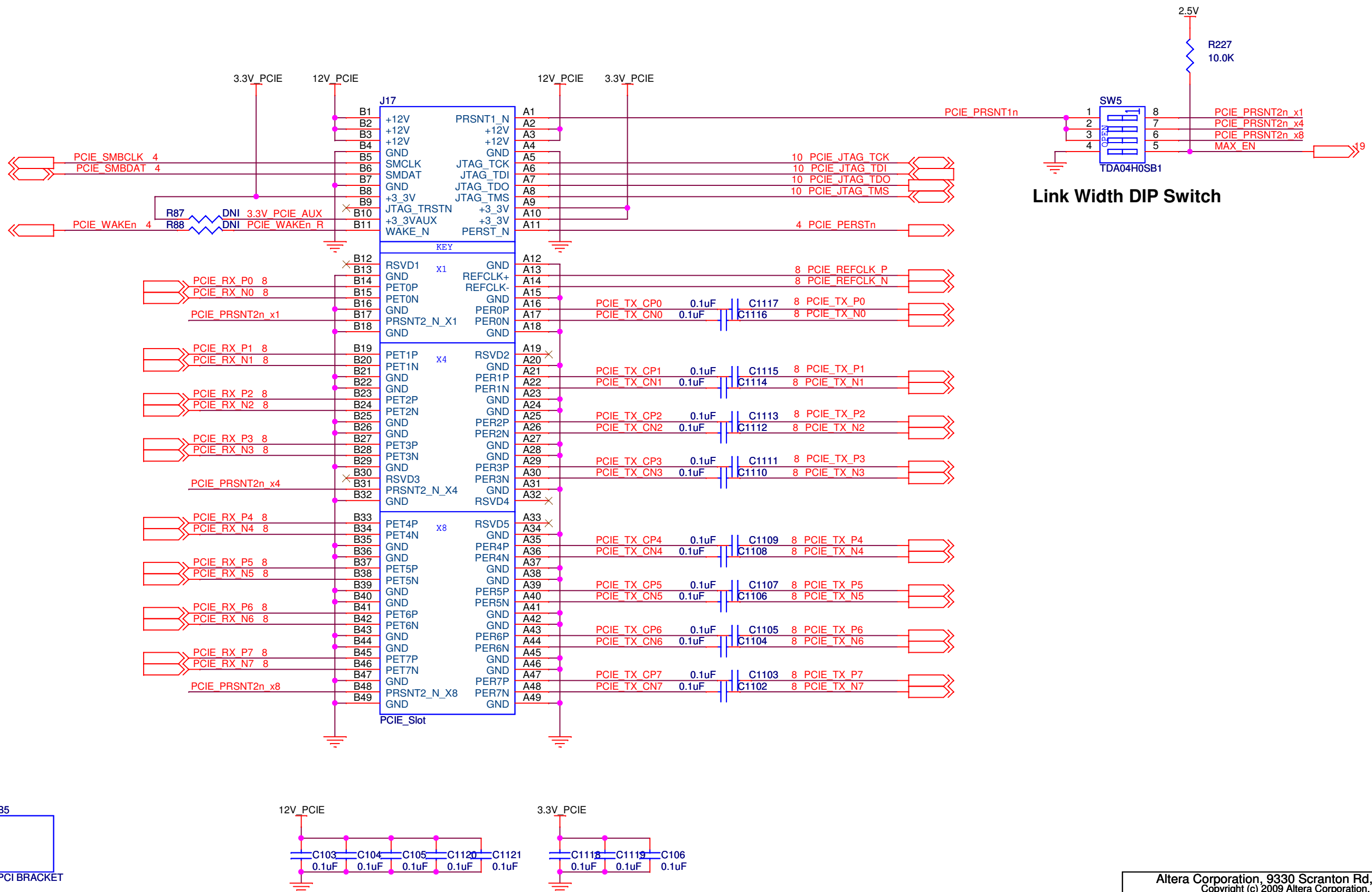
Notes:

- FPGA Schematic Symbol Breakdown:
 - (A) Banks 1A,1C
 - (B) Banks 2A,2C
 - (C) Banks 3A,3B,3C
 - (D) Banks 4A,4B,4C
 - (E) Banks 5A,5C
 - (F) Banks 6A,6C
 - (G) Banks 7A,7B,7C
 - (H) Banks 8A,8B,8C
 - (I) Clocks
 - (J) Configuration
 - (K) Power
 - (L) IO Power
 - (M) GND1
 - (N) GND2
 - (O) GND3
 - (P) Transceivers
 - (Q) Transceiver Power
- Board can support the EP4SGX230 and EP4SGX530 devices and their hardcopy equivalents

Symbol	Pin Type
	User I/O
	User Assigned I/O
	Filter Assigned I/O
	Unbonded Pad
	Reserved Pin
	DIFF_n
	DIFF_p
	DIFF_n Output
	DIFF_p Output
	DQ
	DQS
	DQSB
	CQ#
	Other PLL
	CLK_n
	CLK_p
	PORSEL
	GX_n
	GX_p
	TEMPDIODE
	MSEL0
	MSEL1
	MSEL2
	CONF_DONE
	DCLK
	nCEO
	nCE
	nCONFIG
	TDI
	TCK
	TMS
	TDO
	TRST
	nSTATUS
	nIO_PLLUP
	Other Dedicated Programming
	VREF
	VCCP/VCCR/VCC1
	VCCA
	VCCIO
	GND
	RREF
	No Connect



PCI Express Edge Connector



Stratix IV Banks 1 and 2

U13A

Stratix IV GX Bank 1

Bank 1A

FSM D3	K30	DQ1L/DIFFIO_TX_L2p	DQ5L/DIFFIO_TX_L8p	L31	FSM D27
FSM D2	J30	DQ1L/DIFFIO_TX_L2n	DQ5L/DIFFIO_TX_L8n	K31	FSM D26
FSM D7	N28	DQ1L/DIFFIO_TX_L3p	DQ5L/DIFFIO_TX_L9p	T28	FSM D31
FSM D6	M28	DQ1L/DIFFIO_TX_L3n	DQ5L/DIFFIO_TX_L9n	R28	FSM D30
FSM D11	J32	DQ2L/DIFFIO_TX_L4p	DQ6L/DIFFIO_TX_L10p	T27	MAX2 WEn
FSM D10	H32	DQ2L/DIFFIO_TX_L4n	DQ6L/DIFFIO_TX_L10n	R27	MAX2 BEn3
FSM D13	C32	DQ2L/DIFFIO_TX_L4p	DQ6L/DIFFIO_TX_L10p	G35	SENSE_ADC F0
FSM D12	B32	DQ2L/DIFFIO_RX_L4n	DQ6L/DIFFIO_RX_L10n	F35	SRAM DQP0
FSM D5	D31	DQS1L/DIFFIO_RX_L2p	DQS5L/DIFFIO_RX_L8p	F32	FSM D29
FSM D4	C31	DQS1L/DIFFIO_RX_L2n	DQS5L/DIFFIO_RX_L8n	E32	FSM D28
FSM D9	D35	DQS2L/DIFFIO_RX_L3p	DQS6L/DIFFIO_RX_L9p	F34	MAX2 BEn1
FSM D8	C35	DQS2L/DIFFIO_RX_L3n	DQS6L/DIFFIO_RX_L9n	E34	MAX2 CSn

FSM D15	N31	DQ3L/DIFFIO_TX_L5p	DQ7L/DIFFIO_TX_L11p	K32	MAX2 CLK
FSM D14	M31	DQ3L/DIFFIO_TX_L5n	DQ7L/DIFFIO_TX_L11n	J33	MAX2 OEn
FSM D19	N30	DQ3L/DIFFIO_TX_L6p	DQ7L/DIFFIO_TX_L12p	R29	PCIE_LED_X1
FSM D18	M30	DQ3L/DIFFIO_TX_L6n	DQ7L/DIFFIO_TX_L12n	P29	MAX2 BEn2
FSM D23	N29	DQ4L/DIFFIO_TX_L7p	DQ8L/DIFFIO_TX_L13p	G33	USER_DIPSW4
FSM D22	M29	DQ4L/DIFFIO_TX_L7n	DQ8L/DIFFIO_TX_L13n	F33	USER_LED0
FSM D25	F31	DQ4L/DIFFIO_RX_L7p	DQS7L/DIFFIO_RX_L11p	L29	ENET_TX_P
FSM D24	E31	DQ4L/DIFFIO_RX_L7n	DQS7L/DIFFIO_RX_L11n	K29	ENET_TX_N

FSM D17	D33	DQS3L/DIFFIO_RX_L5p	DIFFIO_TX_L1p	L29	ENET_TX_P
FSM D16	C33	DQS3L/DIFFIO_RX_L5n	DIFFIO_TX_L1n	K29	ENET_TX_N
FSM D21	H31	DQS4L/DIFFIO_RX_L6p	DIFFIO_RX_L12p	H34	MAX2 BEn0
FSM D20	G31	DQS4L/DIFFIO_RX_L6n	DIFFIO_RX_L12n	H35	SENSE_CS1n

FSM D1	D34	RUP1A/DIFFIO_RX_L1p	DIFFIO_RX_L12n		
FSM D0	C34	RDN1A/DIFFIO_RX_L1n			

Bank 1C

USER_LED5	M32	DQ8L/DIFFIO_TX_L13p	DQ10L/DIFFIO_TX_L16p	R32	PCIE_PERSTn
LCD_DATA3	L32	DQ8L/DIFFIO_TX_L13n	DQ10L/DIFFIO_TX_L16n	R33	
PCIE_WAKEn	P31	DQ8L/DIFFIO_TX_L14p	DQ10L/DIFFIO_TX_L17p	W28	USER_LED2
PCIE_SMBDAT	P32	DQ8L/DIFFIO_TX_L14n	DQ10L/DIFFIO_TX_L17n	V28	SENSE_SDO
SRAM_DQP2	N33	DQ9L/DIFFIO_RX_L15p	DQ11L/DIFFIO_RX_L18p	U31	USER_LED14
USER_LED8	N34	DQ9L/DIFFIO_RX_L15n	DQ11L/DIFFIO_RX_L18n	V31	ENET_RESETEn
LCD_DATA4	T30	DQ9L/DIFFIO_TX_L15p	DQ11L/DIFFIO_TX_L18p	R30	ENET_INTn
LCD_DATA6	T31	DQ9L/DIFFIO_TX_L15n	DQ11L/DIFFIO_TX_L18n		

DIFFIO_TX_L18n on CONFIG BLOCK

USER_DIPSW2	J34	DQS8L/DIFFIO_RX_L13p	DQS10L/DIFFIO_RX_L16p	M33	ENET_MDIO
SENSE_SDI	J35	DQS8L/DIFFIO_RX_L13n	DQS10L/DIFFIO_RX_L16n	M34	USER_PB2
LCD_CSn	K34	DQS9L/DIFFIO_RX_L14p	DQS11L/DIFFIO_RX_L17p	L34	USER_LED3
USER_DIPSW5	K35	DQS9L/DIFFIO_RX_L14n	DQS11L/DIFFIO_RX_L17n	L35	USER_LED6

EP4SGX230KF40_F1517
Version = 0.4 Preliminary

U13B

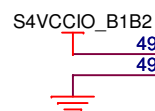
Stratix IV GX Bank 2

Bank 2A

FSM A2	AC26	DQ20L/DIFFIO_TX_L33p	DQ24L/DIFFIO_TX_L39p	AE26	SRAM_CLK
FSM A3	AD26	DQ20L/DIFFIO_TX_L33n	DQ24L/DIFFIO_TX_L39n	AF26	FLASH_CLK
FSM A6	AD27	DQ20L/DIFFIO_TX_L34p	DQ24L/DIFFIO_TX_L40p	AK30	SRAM_BWEn
FSM A7	AE27	DQ20L/DIFFIO_TX_L34n	DQ24L/DIFFIO_TX_L40n	AL30	FLASH_RESETEn
FSM A8	AT34	DQ21L/DIFFIO_RX_L35p	DQ25L/DIFFIO_RX_L41p	AT31	FLASH_WEn
FSM A9	AR34	DQ21L/DIFFIO_RX_L35n	DQ25L/DIFFIO_RX_L41n	AU31	FLASH_CEn
FSM A10	AJ31	DQ21L/DIFFIO_TX_L35p	DQ25L/DIFFIO_TX_L41p	AG28	SRAM_ADSPn
FSM A11	AH30	DQ21L/DIFFIO_TX_L35n	DQ25L/DIFFIO_TX_L41n	AH28	SRAM_BWn2
FSM A4	AN33	DQS20L/DIFFIO_RX_L34p	DQS24L/DIFFIO_RX_L40p	AM31	SRAM_ADSCn
FSM A5	AP34	DQS20L/DIFFIO_RX_L34n	DQS24L/DIFFIO_RX_L40n	AN31	FLASH_ADVn
FSM A12	AT33	DQS21L/DIFFIO_RX_L36p	DQS25L/DIFFIO_RX_L42p	AR31	SRAM_BWn1
FSM A13	AU33	DQS21L/DIFFIO_RX_L36n	DQS25L/DIFFIO_RX_L42n	AT30	SRAM_CEn

FSM A14	AK32	DQ22L/DIFFIO_TX_L36p	DQ26L/DIFFIO_TX_L42p	AG27	FLASH_OEn
FSM A15	AL32	DQ22L/DIFFIO_TX_L36n	DQ26L/DIFFIO_TX_L42n	AH27	SRAM_BWn0
FSM A18	AG29	DQ22L/DIFFIO_TX_L37p	DQ26L/DIFFIO_TX_L43p	AL29	SRAM_BWn3
FSM A19	AH29	DQ22L/DIFFIO_TX_L37n	DQ26L/DIFFIO_TX_L43n	AM29	HSMA_CLK_OUT0
FSM A20	AP32	DQ23L/DIFFIO_RX_L38p	DQS26L/DIFFIO_RX_L43p	AT32	FLASH_RDYBSYn
FSM A21	AR32	DQ23L/DIFFIO_RX_L38n	DQS26L/DIFFIO_RX_L43n	AU32	SRAM_ADVn
FSM A22	AK31	DQ23L/DIFFIO_TX_L38p	DQ23L/DIFFIO_TX_L38n	AN32	FSM_A0
FSM A23	AL31	DQ23L/DIFFIO_TX_L38n	DQ23L/DIFFIO_TX_L38n	AP33	FSM_A1

FSM A16	AP35	DQS22L/DIFFIO_RX_L37p	DIFFIO_RX_L33p	AN32	FSM_A0
FSM A17	AR35	DQS22L/DIFFIO_RX_L37n	DIFFIO_RX_L33n	AP33	FSM_A1
FSM A24	AN30	DQS23L/DIFFIO_RX_L39p	DIFFIO_TX_L44p	AJ29	SRAM_ZZ
FSM A25	AP30	DQS23L/DIFFIO_RX_L39n	DIFFIO_TX_L44n	AK29	HSMB_CLK_OUT0



Bank 2C

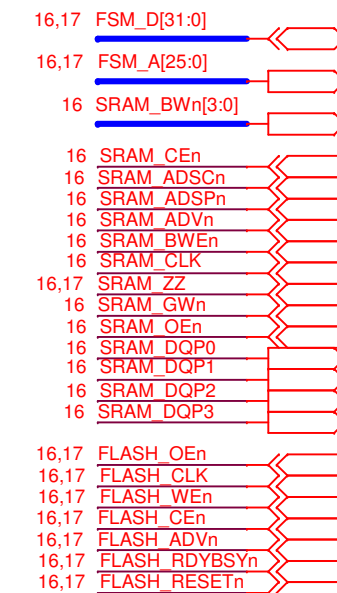
ENET_RX_P	AC31	DQ14L/DIFFIO_RX_L24p	DQ18L/DIFFIO_RX_L30p	AN34	LCD_DATA5
ENET_RX_N	AC32	DQ14L/DIFFIO_RX_L24n	DQ18L/DIFFIO_RX_L30n	AN35	USER_DIPSW3
LCD_D_Cn	AB30	DQ14L/DIFFIO_TX_L24p	DQ18L/DIFFIO_TX_L30p	AD30	LCD_DATA7
SENSE_CS0n	AB31	DQ14L/DIFFIO_TX_L24n	DQ18L/DIFFIO_TX_L30n	AD31	LCD_DATA0
HSMB_SCL	AB27	DQ15L/DIFFIO_TX_L25p	DQ19L/DIFFIO_TX_L31p	AF29	HSMB_SDA
PCIE_LED_G2	AB28	DQ15L/DIFFIO_TX_L25n	DQ19L/DIFFIO_TX_L31n	AG30	USER_LED12
SRAM_GWn	AC28	DQ15L/DIFFIO_TX_L26p	DQ19L/DIFFIO_TX_L32p	AE30	USER_LED10
LCD_DATA1	AJ34	DQ15L/DIFFIO_TX_L26n	DQ19L/DIFFIO_TX_L32n	AE31	PCIE_SMBCLK

SRAM_DQP3	AJ35	DQS14L/DIFFIO_RX_L25p	DQS18L/DIFFIO_RX_L31p	AM34	USER_LED4
ENET_MDC	AH34	DQS14L/DIFFIO_RX_L25n	DQS18L/DIFFIO_RX_L31n	AM35	USER_LED7
PCIE_LED_X4	AH35	DQS15L/DIFFIO_RX_L26p	DQS19L/DIFFIO_RX_L32p	AJ32	SRAM_DQP1
USER_PB0	AK35	DQS15L/DIFFIO_RX_L26n	DQS19L/DIFFIO_RX_L32n	AK33	USER_LED1

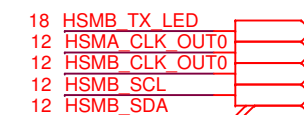
USER_LED13	AD29	DQ16L/DIFFIO_RX_L27n	DQS16L/DIFFIO_RX_L28p	AL34	LCD_WEn
PCIE_LED_X8	AE29	DQ16L/DIFFIO_RX_L27p	DQS16L/DIFFIO_RX_L28n	AL35	USER_DIPSW0
SENSE_SCK	AE28	DQ16L/DIFFIO_TX_L27n	DQS17L/DIFFIO_RX_L29p	AH32	SENSE_SMB_DATA
		DQ16L/DIFFIO_TX_L27p	DQS17L/DIFFIO_RX_L29n	AH33	HSMB_TX_LED

EP4SGX230KF40_F1517
Version = 0.4 Preliminary

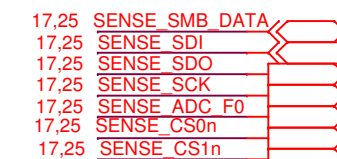
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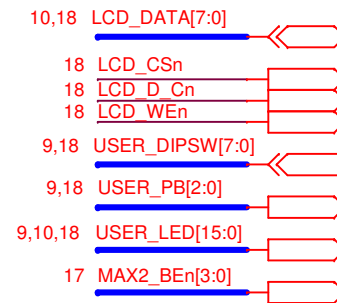
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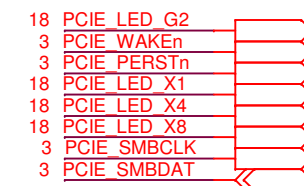
SENSE INTERFACE



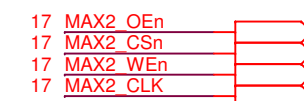
LCD & USER I/O INTERFACES



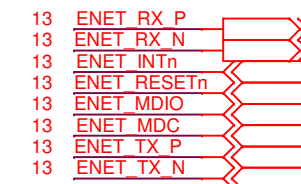
PCIE INTERFACE



MAX II CONTROL



ETHERNET INTERFACE



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Title		
Stratix IV GX FPGA Development Kit Board		
Size	Document Number	Rev
B	150-0310901-B1 (6XX-41284R)	B
Date:	Friday, May 01, 2009	Sheet 4 of 29



Stratix IV Banks 5 and 6

U13E

Stratix IV GX Bank 5

Bank 5A

HSMB D1	AN10	DQ1R/DIFFIO_TX_R2p	DQ5R/DIFFIO_TX_R8p	AK9	HSMA TX D P4	HSMB TX D P15	T13	DQ20R/DIFFIO_TX_R33p	DQ24R/DIFFIO_TX_R39p	K9	HSMB TX D P11
HSMB D0	AP10	DQ1R/DIFFIO_TX_R2n	DQ5R/DIFFIO_TX_R8n	AL9	HSMA TX D N4	HSMB TX D N15	T12	DQ20R/DIFFIO_TX_R33n	DQ24R/DIFFIO_TX_R39n	J9	HSMB TX D N11
SDI_CLK148_DN	AH11	DQ1R/DIFFIO_TX_R3p	DQ5R/DIFFIO_TX_R9p	AL8	HSMA TX D P3	HSMB TX D P12	H7	DQ20R/DIFFIO_TX_R34p	DQ24R/DIFFIO_TX_R40p	K8	HSMB_CLK_OUT_P1
HSMA_SDA	AJ11	DQ1R/DIFFIO_TX_R3n	DQ5R/DIFFIO_TX_R9n	AM8	HSMA TX D N3	HSMB TX D N12	G7	DQ20R/DIFFIO_TX_R34n	DQ24R/DIFFIO_TX_R40n	J8	HSMB_CLK_OUT_N1
HSMA D1	AV10	DQ2R/DIFFIO_RX_R4p	DQ6R/DIFFIO_RX_R10p	AV5	HSMA RX D P4	HSMB RX D P11	G5	DQ21R/DIFFIO_RX_R35p	DQ25R/DIFFIO_RX_R41p	D9	HSMB_PRSENTn
HSMA D0	AW10	DQ2R/DIFFIO_RX_R4n	DQ6R/DIFFIO_RX_R10n	AW4	HSMA RX D N4	HSMB RX D N11	F5	DQ21R/DIFFIO_RX_R35n	DQ25R/DIFFIO_RX_R41n	C9	
HSMA_PRSENTn	AG12	DQ2R/DIFFIO_TX_R4p	DQ6R/DIFFIO_TX_R10p	AH10	HSMA TX D P6	HSMB TX D P16	R13	DQ21R/DIFFIO_TX_R35p	DQ25R/DIFFIO_TX_R41p	M11	
SDI_CLK148_UP	AH12	DQ2R/DIFFIO_TX_R4n	DQ6R/DIFFIO_TX_R10n	AJ10	HSMA TX D N6	HSMB TX D N16	P13	DQ21R/DIFFIO_TX_R35n	DQ25R/DIFFIO_TX_R41n	L11	HSMA_SCL
HSMB D3	AV8	DQS1R/DIFFIO_RX_R2p	DQS5R/DIFFIO_RX_R8p	AT7	HSMA RX D P5	HSMB RX D P12	F7	DQS20R/DIFFIO_RX_R34p	DQS24R/DIFFIO_RX_R40p	D8	HSMB_RX_D_P15
HSMB D2	AW8	DQS1R/DIFFIO_RX_R2n	DQS5R/DIFFIO_RX_R8n	AU7	HSMA RX D N5	HSMB RX D N12	E7	DQS20R/DIFFIO_RX_R34n	DQS24R/DIFFIO_RX_R40n	C8	HSMB_RX_D_N15
HSMB_RX_LED	AT10	DQS2R/DIFFIO_RX_R3p	DQS6R/DIFFIO_RX_R9p	AT6	HSMA RX D P6	HSMB RX D P10	G6	DQS21R/DIFFIO_RX_R36p	DQS25R/DIFFIO_RX_R42p	D5	HSMA_TX_LED
	AU10	DQS2R/DIFFIO_RX_R3n	DQS6R/DIFFIO_RX_R9n	AU6	HSMA RX D N6	HSMB RX D N10	F6	DQS21R/DIFFIO_RX_R36n	DQS25R/DIFFIO_RX_R42n	C5	
HSMA_CLK_OUT_P2	AF13	DQ3R/DIFFIO_TX_R5p	DQ7R/DIFFIO_TX_R11p	AE13	HSMA TX D P2	HSMB TX D P14	R12	DQ22R/DIFFIO_TX_R36p	DQ26R/DIFFIO_TX_R42p	N12	
HSMA_CLK_OUT_N2	AG13	DQ3R/DIFFIO_TX_R5n	DQ7R/DIFFIO_TX_R11n	AE12	HSMA TX D N2	HSMB TX D N14	R11	DQ22R/DIFFIO_TX_R36n	DQ26R/DIFFIO_TX_R42n	M12	
HSMA_TX_D_P0	AN9	DQ3R/DIFFIO_TX_R6p	DQ7R/DIFFIO_TX_R12p	AD13	HSMA TX D P13	HSMB TX D P7	N11	DQ22R/DIFFIO_TX_R37p	DQ26R/DIFFIO_TX_R43p	K10	HSMB_CLK_OUT_P2
HSMA_TX_D_N0	AP9	DQ3R/DIFFIO_TX_R6n	DQ7R/DIFFIO_TX_R12n	AD12	HSMA TX D N13	HSMB TX D N7	N10	DQ22R/DIFFIO_TX_R37n	DQ26R/DIFFIO_TX_R43n	J10	HSMB_CLK_OUT_N2
HSMA_RX_D_P2	AP8	DQ4R/DIFFIO_RX_R7p		AR5	HSMA RX D P7	HSMB RX D P16	F10	DQ23R/DIFFIO_RX_R38p		D10	
HSMA_RX_D_N2	AR8	DQ4R/DIFFIO_RX_R7n	DQS7R/DIFFIO_RX_R11p	AT5	HSMA RX D N7	HSMB RX D N16	E10	DQ23R/DIFFIO_RX_R38n	DQS26R/DIFFIO_RX_R43p	C10	
HSMA_TX_D_P1	AN7	DQ4R/DIFFIO_TX_R7p	DQS7R/DIFFIO_RX_R11p			HSMB TX D P13	M10	DQ23R/DIFFIO_TX_R38p	DQS26R/DIFFIO_RX_R43n		
HSMA_TX_D_N1	AP7	DQ4R/DIFFIO_TX_R7n	DQS7R/DIFFIO_RX_R11n			HSMB TX D N13	L10	DQ23R/DIFFIO_TX_R38n			
HSMA_RX_D_P0	AT9	DQS3R/DIFFIO_RX_R5p	RUP5A/DIFFIO_RX_R1p	AV7	HSMA D3	HSMB RX D P13	G9	DQS22R/DIFFIO_RX_R37p	DIFFIO_RX_R33p	G8	HSMB_RX_D_P9
HSMA_RX_D_N0	AU9	DQS3R/DIFFIO_RX_R5n	RDN5A/DIFFIO_RX_R1n	AW7	HSMA D2	HSMB RX D N13	F9	DQS22R/DIFFIO_RX_R37n	DIFFIO_RX_R33n	F8	HSMB_RX_D_N9
HSMA_RX_D_P1	AT8	DQS4R/DIFFIO_RX_R6p	DIFFIO_TX_R1p	AL10	HSMA_CLK_OUT_P1	HSMB RX D P14	D7	DQS23R/DIFFIO_RX_R39p	DIFFIO_TX_R44p	H10	
HSMA_RX_D_N1	AU8	DQS4R/DIFFIO_RX_R6n	DIFFIO_RX_R12p	AM10	HSMA_CLK_OUT_N1	HSMB RX D N14	C7	DQS23R/DIFFIO_RX_R39n	DIFFIO_TX_R44n	G10	
			DIFFIO_RX_R12n	AW6	HSMA RX D P3				RUP6A/DIFFIO_RX_R44p	D6	
				AW5	HSMA RX D N3				RDN6A/DIFFIO_RX_R44n	C6	HSMA_RX_LED

Bank 5C

HSMA_TX_D_P7	AH9	DQ8R/DIFFIO_TX_R13p	DQ12R/DIFFIO_TX_R19p	AG8	HSMA TX D P8	HSMB TX D P1	V12	DQ14R/DIFFIO_TX_R24p	DQ18R/DIFFIO_RX_R30p	N8	HSMB_RX_D_P5
HSMA_TX_D_N7	AH8	DQ8R/DIFFIO_TX_R13n	DQ12R/DIFFIO_TX_R19n	AG7	HSMA TX D N8	HSMB TX D N1	V11	DQ14R/DIFFIO_TX_R24n	DQ18R/DIFFIO_RX_R30n	N7	HSMB_RX_D_N5
HSMA_TX_D_P5	AK8	DQ8R/DIFFIO_TX_R14p	DQ12R/DIFFIO_TX_R20p	AB11	HSMA TX D P15	HSMB RX D P0	W8	DQ14R/DIFFIO_TX_R24p	DQ18R/DIFFIO_TX_R30p	M8	HSMB_TX_D_P8
HSMA_TX_D_N5	AK7	DQ8R/DIFFIO_TX_R14n	DQ12R/DIFFIO_TX_R20n	AB10	HSMA TX D N15	HSMB RX D N0	W7	DQ14R/DIFFIO_TX_R24n	DQ18R/DIFFIO_TX_R30n	M7	HSMB_TX_D_N8
HSMA_RX_D_P9	AN6	DQ9R/DIFFIO_RX_R15p	DQ13R/DIFFIO_RX_R21p	AG6	HSMA RX D P15	HSMB TX D P3	U10	DQ15R/DIFFIO_TX_R25p	DQ19R/DIFFIO_TX_R31p	L8	HSMB_TX_D_P9
HSMA_RX_D_N9	AN5	DQ9R/DIFFIO_RX_R15n	DQ13R/DIFFIO_RX_R21n	AG5	HSMA RX D N15	HSMB TX D N3	T9	DQ15R/DIFFIO_TX_R25n	DQ19R/DIFFIO_TX_R31n	L7	HSMB_TX_D_N9
HSMA_TX_D_P12	AE11	DQ9R/DIFFIO_TX_R15p	DQ13R/DIFFIO_TX_R21p	AB13	HSMA TX D P14	HSMB TX D P2	V10	DQ15R/DIFFIO_TX_R26p	DQ19R/DIFFIO_TX_R32p	K7	HSMB_TX_D_P10
HSMA_TX_D_N12	AE10	DQ9R/DIFFIO_TX_R15n	DQ13R/DIFFIO_TX_R21n	AB12	HSMA TX D N14	HSMB TX D N2	V9	DQ15R/DIFFIO_TX_R26n	DQ19R/DIFFIO_TX_R32n	J7	HSMB_TX_D_N10
HSMA_RX_D_P8	AP6	DQS8R/DIFFIO_RX_R13p	DQS12R/DIFFIO_RX_R19p	AB9	HSMA RX D P16	HSMB RX D P1	V6	DQS14R/DIFFIO_RX_R25p	DQS18R/DIFFIO_RX_R31p	K6	HSMB_RX_D_P7
HSMA_RX_D_N8	AP5	DQS8R/DIFFIO_RX_R13n	DQS12R/DIFFIO_RX_R19n	AC8	HSMA RX D N16	HSMB RX D N1	U5	DQS14R/DIFFIO_RX_R25n	DQS18R/DIFFIO_RX_R31n	K5	HSMB_RX_D_N7
HSMA_RX_D_P10	AM6	DQS9R/DIFFIO_RX_R14p	DQS13R/DIFFIO_RX_R20p	AH6	HSMA RX D P14	HSMB RX D P3	R6	DQS15R/DIFFIO_RX_R26p	DQS19R/DIFFIO_RX_R32p	J6	HSMB_RX_D_P8
HSMA_RX_D_N10	AM5	DQS9R/DIFFIO_RX_R14n	DQS13R/DIFFIO_RX_R20n	AH5	HSMA RX D N14	HSMB RX D N3	R5	DQS15R/DIFFIO_RX_R26n	DQS19R/DIFFIO_RX_R32n	J5	HSMB_RX_D_N8
HSMA_TX_D_P10	AF11	DQ10R/DIFFIO_TX_R16p				HSMB RX D P2	R7	DQ16R/DIFFIO_RX_R27p			
HSMA_TX_D_N10	AF10	DQ10R/DIFFIO_TX_R16n				HSMB RX D N2	P6	DQ16R/DIFFIO_RX_R27n			
HSMA_TX_D_P9	AG10	DQ10R/DIFFIO_TX_R17p				HSMB TX D P6	N9	DQ16R/DIFFIO_TX_R27p			
HSMA_TX_D_N9	AG9	DQ10R/DIFFIO_TX_R17n				HSMB TX D N6	P8	DQ16R/DIFFIO_TX_R27n			
HSMA_RX_D_P13	AJ6	DQ11R/DIFFIO_RX_R18p				HSMB TX D P4	T10	DQ17R/DIFFIO_TX_R28p			
HSMA_RX_D_N13	AJ5	DQ11R/DIFFIO_RX_R18n				HSMB TX D N4	R10	DQ17R/DIFFIO_TX_R28n			
HSMA_TX_D_P11	AD10	DQ11R/DIFFIO_TX_R18p				HSMB TX D P5	R9	DQ17R/DIFFIO_TX_R29p			
HSMA_TX_D_N11	AD9	DQ11R/DIFFIO_TX_R18n				HSMB TX D N5	R8	DQ17R/DIFFIO_TX_R29n			
HSMA_RX_D_P11	AL6	DQS10R/DIFFIO_RX_R16p				HSMB RX D P4	N6	DQS16R/DIFFIO_RX_R28p			
HSMA_RX_D_N11	AL5	DQS10R/DIFFIO_RX_R16n				HSMB RX D N4	N5	DQS16R/DIFFIO_RX_R28n			
HSMA_RX_D_P12	AK6	DQS11R/DIFFIO_RX_R17p				HSMB RX D P6	M6	DQS17R/DIFFIO_RX_R29p			
HSMA_RX_D_N12	AK5	DQS11R/DIFFIO_RX_R17n				HSMB RX D N6	L5	DQS17R/DIFFIO_RX_R29n			

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Stratix IV GX Bank 6

Bank 6A

HSMB TX D P15	T13	DQ20R/DIFFIO_TX_R33p	DQ24R/DIFFIO_TX_R39p	K9	HSMB TX D P11
HSMB TX D N15	T12	DQ20R/DIFFIO_TX_R33n	DQ24R/DIFFIO_TX_R39n	J9	HSMB TX D N11
HSMB TX D P12	H7	DQ20R/DIFFIO_TX_R34p	DQ24R/DIFFIO_TX_R40p	K8	HSMB_CLK_OUT_P1
HSMB TX D N12	G7	DQ20R/DIFFIO_TX_R34n	DQ24R/DIFFIO_TX_R40n	J8	HSMB_CLK_OUT_N1
HSMB RX D P11	G5	DQ21R/DIFFIO_RX_R35p	DQ25R/DIFFIO_RX_R41p	D9	HSMB_PRSENTn
HSMB RX D N11	F5	DQ21R/DIFFIO_RX_R35n	DQ25R/DIFFIO_RX_R41n	C9	
HSMB TX D P16	R13	DQ21R/DIFFIO_TX_R35p	DQ25R/DIFFIO_TX_R41p	M11	
HSMB TX D N16	P13	DQ21R/DIFFIO_TX_R35n	DQ25R/DIFFIO_TX_R41n	L11	HSMA_SCL
HSMB RX D P12	F7	DQS20R/DIFFIO_RX_R34p	DQS24R/DIFFIO_RX_R40p	D8	HSMB_RX_D_P15
HSMB RX D N12	E7	DQS20R/DIFFIO_RX_R34n	DQS24R/DIFFIO_RX_R40n	C8	HSMB_RX_D_N15
HSMB RX D P10	G6	DQS21R/DIFFIO_RX_R36p	DQS25R/DIFFIO_RX_R42p	D5	HSMA_TX_LED
HSMB RX D N10	F6	DQS21R/DIFFIO_RX_R36n	DQS25R/DIFFIO_RX_R42n	C5	
HSMB TX D P14	R12	DQ22R/DIFFIO_TX_R36p	DQ26R/DIFFIO_TX_R42p	N12	
HSMB TX D N14	R11	DQ22R/DIFFIO_TX_R36n	DQ26R/DIFFIO_TX_R42n	M12	
HSMB TX D P7	N11	DQ22R/DIFFIO_TX_R37p	DQ26R/DIFFIO_TX_R43p	K10	HSMB_CLK_OUT_P2
HSMB TX D N7	N10	DQ22R/DIFFIO_TX_R37n	DQ26R/DIFFIO_TX_R43n	J10	HSMB_CLK_OUT_N2
HSMB RX D P16	F10	DQ23R/DIFFIO_RX_R38p		D10	
HSMB RX D N16	E10	DQ23R/DIFFIO_RX_R38n	DQS26R/DIFFIO_RX_R43p	C10	
HSMB TX D P13	M10	DQ23R/DIFFIO_TX_R38p	DQS26R/DIFFIO_RX_R43n		
HSMB TX D N13	L10	DQ23R/DIFFIO_TX_R38n			
HSMB RX D P13	G9	DQS22R/DIFFIO_RX_R37p	DIFFIO_RX_R33p	G8	HSMB_RX_D_P9
HSMB RX D N13	F9	DQS22R/DIFFIO_RX_R37n	DIFFIO_RX_R33n	F8	HSMB_RX_D_N9
HSMB RX D P14	D7	DQS23R/DIFFIO_RX_R39p	DIFFIO_TX_R44p	H10	
HSMB RX D N14	C7	DQS23R/DIFFIO_RX_R39n	DIFFIO_TX_R44n	G10	

Bank 6C

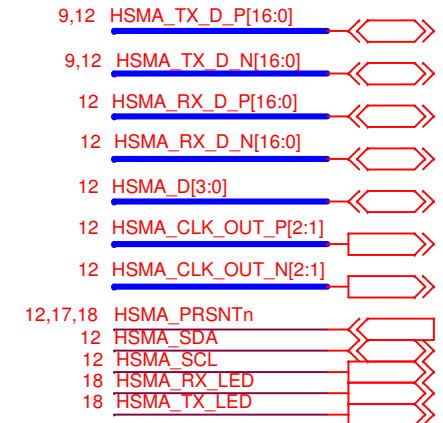
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HSMB TX D N1	V11	DQ14R/DIFFIO_TX_R24n	DQ18R/DIFFIO_RX_R30n	N7	HSMB_RX_D_N5
HSMB RX D P0	W8	DQ14R/DIFFIO_TX_R24p	DQ18R/DIFFIO_TX_R30p	M8	HSMB_TX_D_P8
HSMB RX D N0	W7	DQ14R/DIFFIO_TX_R24n	DQ18R/DIFFIO_TX_R30n	M7	HSMB_TX_D_N8
HSMB TX D P3	U10	DQ15R/DIFFIO_TX_R25p	DQ19R/DIFFIO_TX_R31p	L8	HSMB_TX_D_P9
HSMB TX D N3	T9	DQ15R/DIFFIO_TX_R25n	DQ19R/DIFFIO_TX_R31n	L7	HSMB_TX_D_N9
HSMB TX D P2	V10	DQ15R/DIFFIO_TX_R26p	DQ19R/DIFFIO_TX_R32p	K7	HSMB_TX_D_P10
HSMB TX D N2	V9	DQ15R/DIFFIO_TX_R26n	DQ19R/DIFFIO_TX_R32n	J7	HSMB_TX_D_N10
HSMB RX D P1	V6	DQS14R/DIFFIO_RX_R25p	DQS18R/DIFFIO_RX_R31p	K6	HSMB_RX_D_P7
HSMB RX D N1	U5	DQS14R/DIFFIO_RX_R25n	DQS18R/DIFFIO_RX_R31n	K5	HSMB_RX_D_N7
HSMB RX D P3	R6	DQS15R/DIFFIO_RX_R26p	DQS19R/DIFFIO_RX_R32p	J6	HSMB_RX_D_P8
HSMB RX D N3	R5	DQS15R/DIFFIO_RX_R26n	DQS19R/DIFFIO_RX_R32n	J5	HSMB_RX_D_N8
HSMB RX D P2	R7	DQ16R/DIFFIO_RX_R27p			
HSMB RX D N2	P6	DQ16R/DIFFIO_RX_R27n			
HSMB TX D P6	N9	DQ16R/DIFFIO_TX_R27p			
HSMB TX D N6	P8	DQ16R/DIFFIO_TX_R27n			
HSMB TX D P4	T10	DQ17R/DIFFIO_TX_R28p			
HSMB TX D N4	R10	DQ17R/DIFFIO_TX_R28n			
HSMB TX D P5	R9	DQ17R/DIFFIO_TX_R29p			
HSMB TX D N5	R8	DQ17R/DIFFIO_TX_R29n			
HSMB RX D P4	N6	DQS16R/DIFFIO_RX_R28p			
HSMB RX D N4	N5	DQS16R/DIFFIO_RX_R28n			
HSMB RX D P6	M6	DQS17R/DIFFIO_RX_R29p			
HSMB RX D N6	L5	DQS17R/DIFFIO_RX_R29n			

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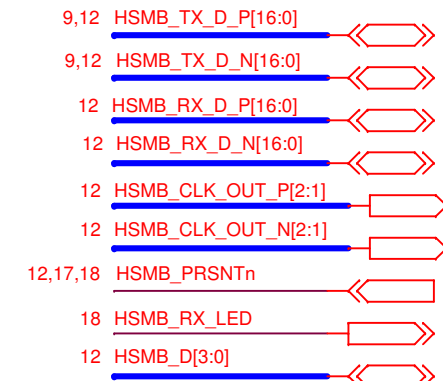
SDI INTERFACE



HSMC PORT A INTERFACE



HSMC PORT B INTERFACE



Stratix IV Banks 7 and 8

U13G

Stratix IV GX Bank 7

Bank 7A

QDR2TOP1 Q17	N13	DQ1T/DIFFOUT_T1p	DQ5T/DIFFOUT_T13p
QDR2TOP1 Q11	M13	DQ1T/DIFFOUT_T1n	DQ5T/DIFFOUT_T13n
QDR2TOP1 Q15	R14	DQ1T/DIFFOUT_T3p	DQ5T/DIFFOUT_T15p
QDR2TOP1 Q16	N15	DQ1T/DIFFOUT_T3n	DQ5T/DIFFOUT_T15n
QDR2TOP1 Q13	M14	DQ2T/DIFFOUT_T5p	DQ6T/DIFFOUT_T17p
QDR2TOP1 Q3	K12	DQ2T/DIFFOUT_T5n	DQ6T/DIFFOUT_T17n
QDR2TOP1 Q9	L14	DQ2T/DIFFIO_RX_T3p	DQ6T/DIFFIO_RX_T9p
QDR2TOP1 Q10	K14	DQ2T/DIFFIO_RX_T3n	DQ6T/DIFFIO_RX_T9n
QDR2TOP1 Q14	P14	RUP7A/DQS1T/DIFFIO_RX_T1p	DQS5T/DIFFIO_RX_T7p
QDR2TOP1 Q12	N14	RDN7A/DQSn1T/DIFFIO_RX_T1n	DQSn5T/DIFFIO_RX_T7n
QDR2TOP1 CQ_N	L13	DQS2T/DIFFIO_RX_T2p	DQS6T/DIFFIO_RX_T8p
QDR2TOP1 Q1	K13	DQS2T/DIFFIO_RX_T2n	DQS6T/DIFFIO_RX_T8n
QDR2TOP1 Q2	J12	DQ3T/DIFFOUT_T7p	DIFFIO_RX_T10p
QDR2TOP1 Q0	J13	DQ3T/DIFFOUT_T7n	DIFFIO_RX_T10n
QDR2TOP1 Q4	H14	DQ3T/DIFFOUT_T9p	DIFFOUT_T19p
QDR2TOP1 Q5	G14	DQ3T/DIFFOUT_T9n	DIFFOUT_T19n
QDR2TOP1 Q6	F12	DQ4T/DIFFOUT_T11p	
QDR2TOP1 QVLD	D13	DQ4T/DIFFOUT_T11n	
QDR2TOP1 Q7	F14	DQ4T/DIFFIO_RX_T6p	
QDR2TOP1 Q8	E14	DQ4T/DIFFIO_RX_T6n	
QDR2TOP1 CQ_P	H13	DQS3T/DIFFIO_RX_T4p	
	G13	DQS3T/DIFFIO_RX_T4n	
	F13	DQS4T/DIFFIO_RX_T5p	
	E13	DQS4T/DIFFIO_RX_T5n	

Bank 7B

QDR2TOP1 D15	E16	DQ7T/DIFFOUT_T21p	DQ9T/DIFFOUT_T27p
QDR2TOP1 D17	G15	DQ7T/DIFFOUT_T21n	DQ9T/DIFFOUT_T27n
QDR2TOP1 D16	F15	DQ7T/DIFFOUT_T23p	DQ9T/DIFFOUT_T29p
QDR2TOP1 D8	G17	DQ7T/DIFFOUT_T23n	DQ9T/DIFFOUT_T29n
QDR2TOP1 D14	D16	DQ8T/DIFFOUT_T25p	DQ10T/DIFFOUT_T31p
QDR2TOP1 D10	A16	DQ8T/DIFFOUT_T25n	DQ10T/DIFFOUT_T31n
QDR2TOP1 D12	C16	DQ8T/DIFFIO_RX_T13p	DQ10T/DIFFIO_RX_T16p
QDR2TOP1 D11	B16	DQ8T/DIFFIO_RX_T13n	DQ10T/DIFFIO_RX_T16n
QDR2TOP1 D9	G16	DQS7T/DIFFIO_RX_T11p	DQS9T/DIFFIO_RX_T14p
QDR2TOP1 A10	F16	DQSn7T/DIFFIO_RX_T11n	DQSn9T/DIFFIO_RX_T14n
DDR3TOP CSn	D15	DQS8T/DIFFIO_RX_T12p	DQS10T/DIFFIO_RX_T15p
QDR2TOP1 D13	C15	DQS8T/DIFFIO_RX_T12n	DQS10T/DIFFIO_RX_T15n

Bank 7C

QDR2TOP1 A11	F17	DQ11T/DIFFOUT_T33p	DQ13T/DIFFOUT_T39p
QDR2TOP1 A0	C17	DQ11T/DIFFOUT_T33n	DQ13T/DIFFOUT_T39n
QDR2TOP1 WPSn	D18	DQ11T/DIFFOUT_T35p	DQ13T/DIFFOUT_T41p
QDR2TOP1 A4	C18	DQ11T/DIFFOUT_T35n	DQ13T/DIFFOUT_T41n
QDR2TOP1 A19	F20	DQ12T/DIFFOUT_T37p	DQS13T/DIFFIO_RX_T20p
QDR2TOP1 A17	G20	DQ12T/DIFFOUT_T37n	DQSn13T/DIFFIO_RX_T20n
QDR2TOP1 A5	G19	DQ12T/DIFFIO_RX_T19p	
QDR2TOP1 RPSn	F19	DQ12T/DIFFIO_RX_T19n	
QDR2TOP1 A16	E17	DQS11T/DIFFIO_RX_T17p	DIFFIO_RX_T21p
QDR2TOP1 A8	D17	DQSn11T/DIFFIO_RX_T17n	DIFFIO_RX_T21n
QDR2TOP1 A7	G18	DQS12T/DIFFIO_RX_T18p	DIFFIO_RX_T22p
QDR2TOP1 A12	F18	DQSn12T/DIFFIO_RX_T18n	DIFFIO_RX_T22n

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Stratix IV GX Bank 8

Bank 8A

QDR2TOP0 RPSn	C27	DQ21T/DIFFOUT_T80p	DQ25T/DIFFOUT_T92p
QDR2TOP0 A5	D27	DQ21T/DIFFOUT_T80n	DQ25T/DIFFOUT_T92n
QDR2TOP0 A19	A28	DQ21T/DIFFIO_RX_T40p	DQ25T/DIFFIO_RX_T46p
QDR2TOP0 A3	A27	DQ21T/DIFFIO_RX_T40n	DQ25T/DIFFIO_RX_T46n
QDR2TOP0 A7	B31	DQ22T/DIFFOUT_T82p	DQ26T/DIFFOUT_T94p
QDR2TOP0 A10	A31	DQ22T/DIFFOUT_T82n	DQ26T/DIFFOUT_T94n
QDR2TOP0 A14	C29	DQ22T/DIFFOUT_T84p	DQ26T/DIFFOUT_T96p
QDR2TOP0 A15	C30	DQ22T/DIFFOUT_T84n	DQ26T/DIFFOUT_T96n
QDR2TOP0 A17	C28	DQS21T/DIFFIO_RX_T41p	DQS25T/DIFFIO_RX_T47p
QDR2TOP0 A13	B28	DQSn21T/DIFFIO_RX_T41n	DQSn25T/DIFFIO_RX_T47n
QDR2TOP0 A6	B29	DQS22T/DIFFIO_RX_T42p	RUP8A/DQS26T/DIFFIO_RX_T48p
QDR2TOP0 A9	A29	DQSn22T/DIFFIO_RX_T42n	RDN8A/DQSn26T/DIFFIO_RX_T48n
QDR2TOP0 Q11	D28	DQ23T/DIFFOUT_T86p	DIFFIO_RX_T39p
QDR2TOP0 Q12	F27	DQ23T/DIFFOUT_T86n	DIFFIO_RX_T39n
QDR2TOP0 Q7	F28	DQ23T/DIFFIO_RX_T43p	DIFFOUT_T78p
QDR2TOP0 Q10	E28	DQ23T/DIFFIO_RX_T43n	DIFFOUT_T78n
QDR2TOP0 Q13	G27	DQ24T/DIFFOUT_T88p	
QDR2TOP0 QVLD	H26	DQ24T/DIFFOUT_T88n	
QDR2TOP0 Q5	J26	DQ24T/DIFFOUT_T90p	
QDR2TOP0 Q6	G29	DQ24T/DIFFOUT_T90n	
QDR2TOP0 Q8	E29	DQS23T/DIFFIO_RX_T44p	
QDR2TOP0 Q9	D29	DQSn23T/DIFFIO_RX_T44n	
QDR2TOP0 CQ_P	H28	DQS24T/DIFFIO_RX_T45p	
QDR2TOP0 A16	G28	DQSn24T/DIFFIO_RX_T45n	

Bank 8B

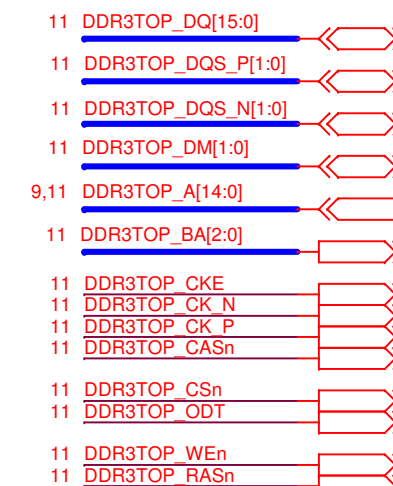
QDR2TOP0 BWSn1	J25	DQ17T/DIFFOUT_T66n	DQ19T/DIFFOUT_T72n
QDR2TOP0 D14	M24	DQ17T/DIFFOUT_T66p	DQ19T/DIFFOUT_T72p
QDR2TOP0 WPSn	K24	DQ17T/DIFFIO_RX_T33p	DQ19T/DIFFIO_RX_T36p
QDR2TOP0 A18	J24	DQ17T/DIFFIO_RX_T33n	DQ19T/DIFFIO_RX_T36n
QDR2TOP0 D12	M23	DQ18T/DIFFOUT_T68n	DQ20T/DIFFOUT_T74n
QDR2TOP0 D10	N22	DQ18T/DIFFOUT_T68p	DQ20T/DIFFOUT_T74p
QDR2TOP0 D9	P22	DQ18T/DIFFOUT_T70n	DQ20T/DIFFOUT_T76n
QDR2TOP0 D11	R22	DQ18T/DIFFOUT_T70p	DQ20T/DIFFOUT_T76p
QDR2TOP0 BWSn0	L23	DQS17T/DIFFIO_RX_T34p	DQS19T/DIFFIO_RX_T37p
QDR2TOP0 D13	K23	DQSn17T/DIFFIO_RX_T34n	DQSn19T/DIFFIO_RX_T37n
QDR2TOP0 K_P	P23	DQS18T/DIFFIO_RX_T35p	DQS20T/DIFFIO_RX_T38p
QDR2TOP0 K_N	N23	DQSn18T/DIFFIO_RX_T35n	DQSn20T/DIFFIO_RX_T38n

Bank 8C

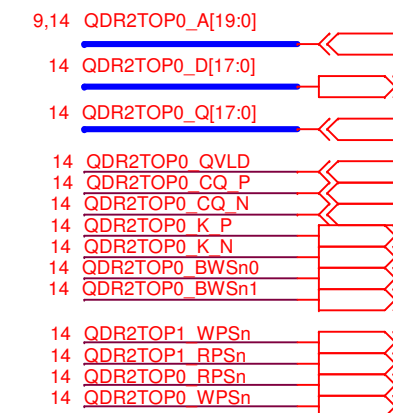
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DDR3TOP A3	R20	DQ14T/DIFFOUT_T56n	DQ16T/DIFFOUT_T62n
QDR2TOP0 A0	N21	DQ14T/DIFFOUT_T58p	DQ16T/DIFFOUT_T64p
DDR3TOP A13	M22	DQ14T/DIFFOUT_T58n	DQ16T/DIFFOUT_T64n
DDR3TOP DQ12	G22	DQ15T/DIFFOUT_T60p	
DDR3TOP DQ8	K22	DQ15T/DIFFOUT_T60n	
DDR3TOP DQ10	J22	DQ15T/DIFFIO_RX_T30p	DQS16T/DIFFIO_RX_T32p
DDR3TOP DQ14	H22	DQ15T/DIFFIO_RX_T30n	DQSn16T/DIFFIO_RX_T32n
DDR3TOP CK_P	D24	DQS14T/DIFFIO_RX_T29p	DIFFIO_RX_T27p
DDR3TOP CK_N	C24	DQSn14T/DIFFIO_RX_T29n	DIFFIO_RX_T27n
DDR3TOP DQS_P1	J23	DQS15T/DIFFIO_RX_T31p	DIFFIO_RX_T28p
DDR3TOP DQS_N1	H23	DQSn15T/DIFFIO_RX_T31n	DIFFIO_RX_T28n

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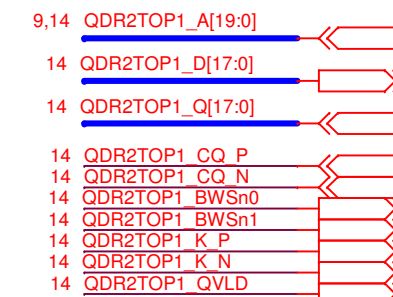
DDR3 TOP INTERFACE



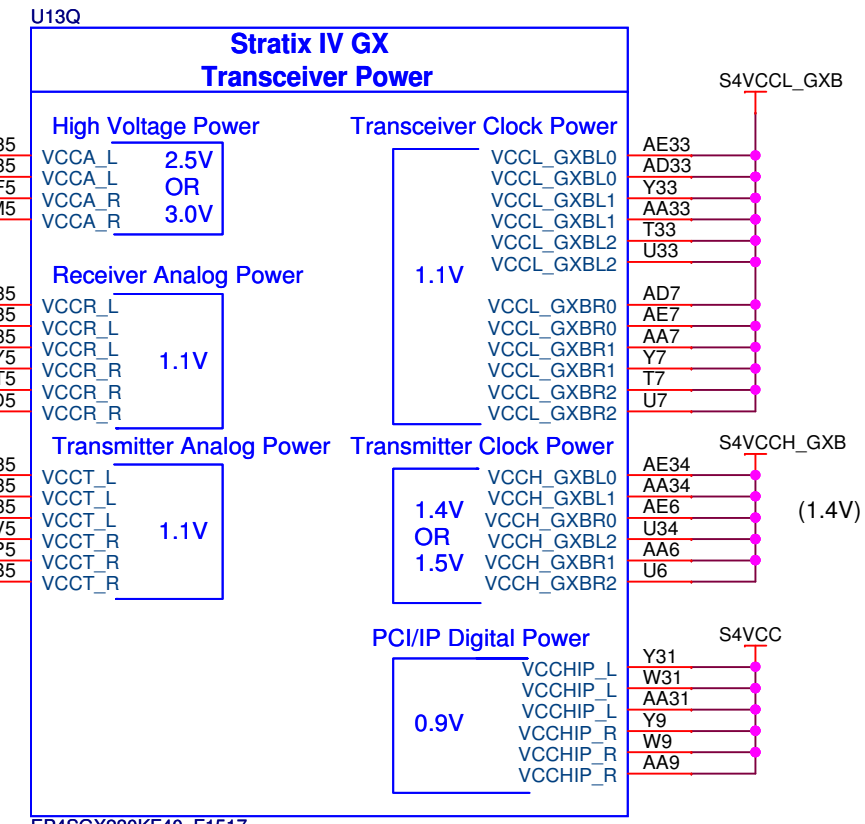
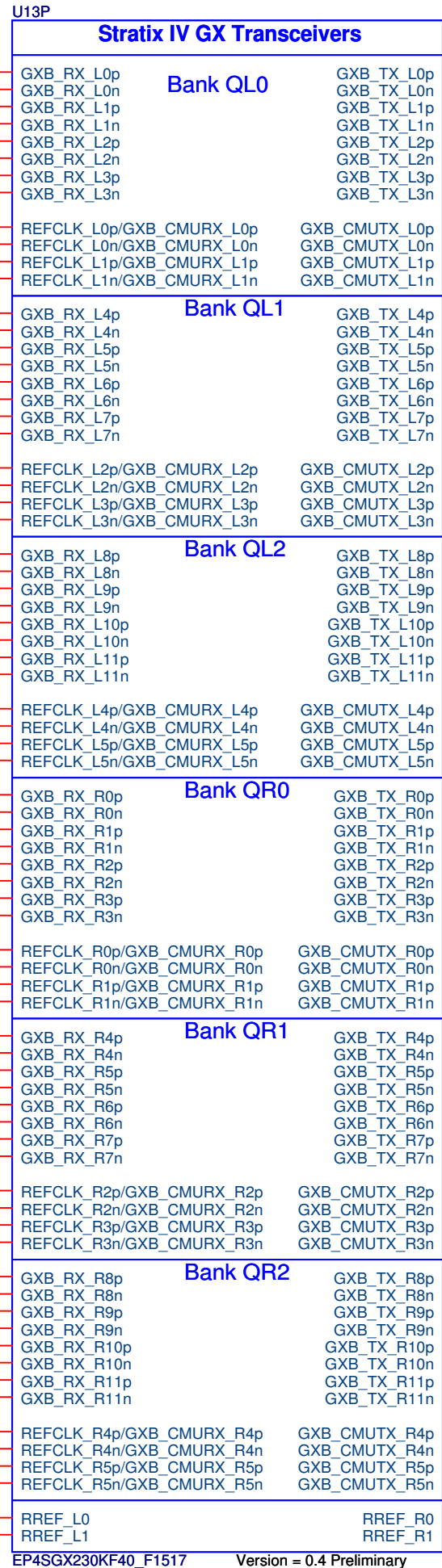
QDRII TOP0 INTERFACE



QDRII TOP1 INTERFACE



Stratix IV GX Transceivers I/O and Power



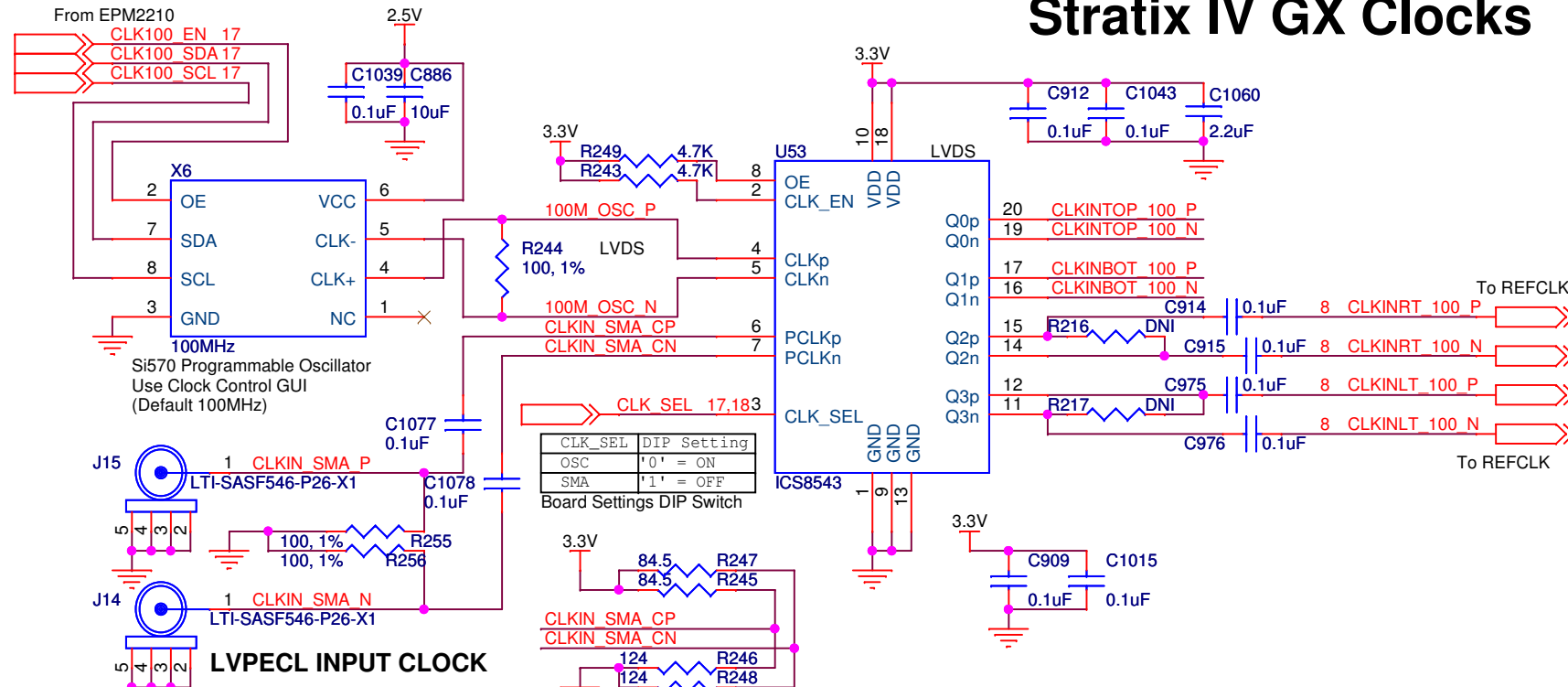
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Version = 0.4 Preliminary



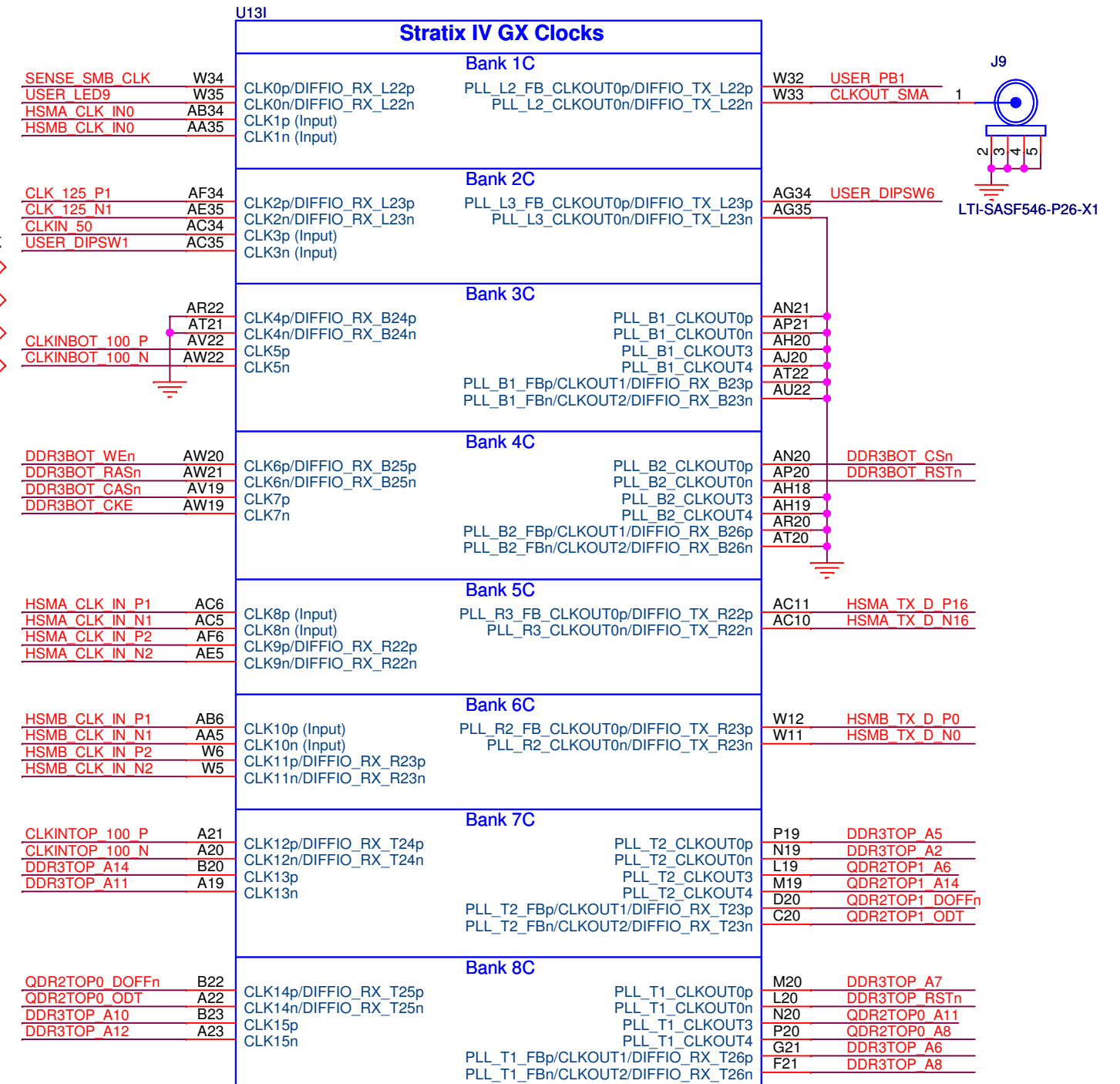
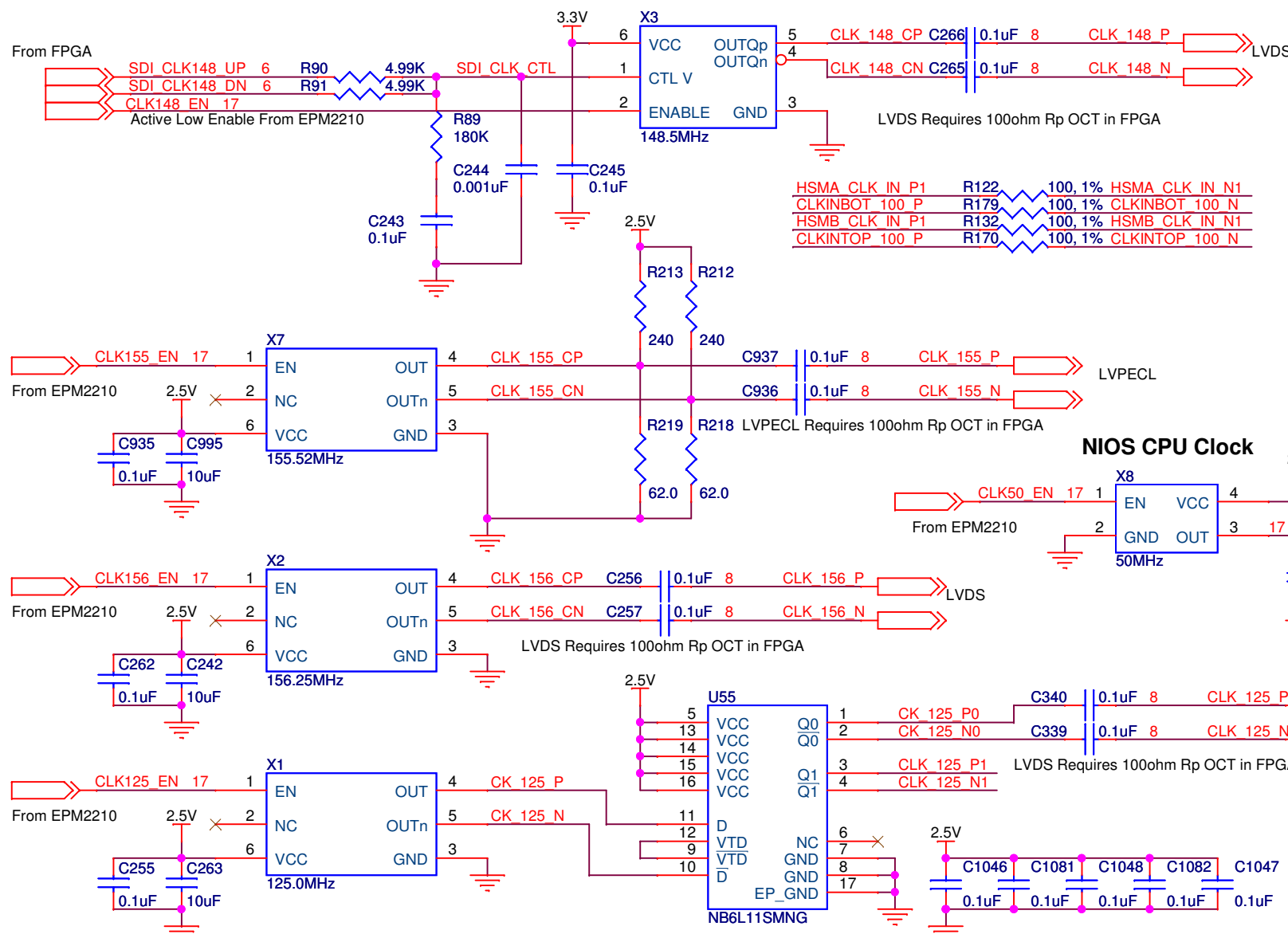
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EP4SGX230KF40_F1517 Version = 0.4 Preliminary

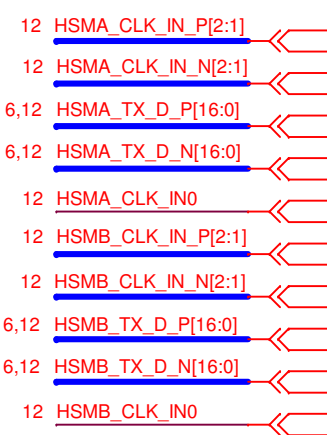
Stratix IV GX Clocks



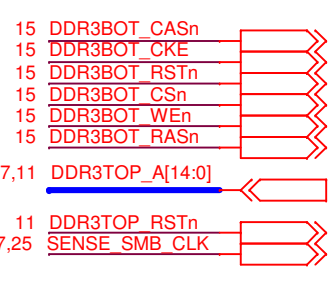
Dedicated GX Reference Clocks



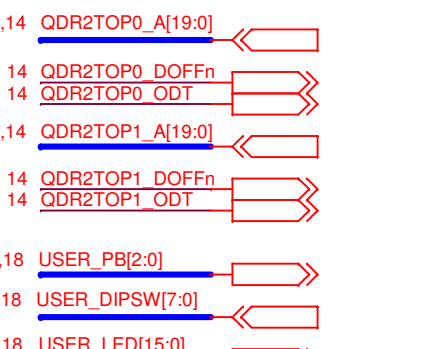
HSM INTERFACE



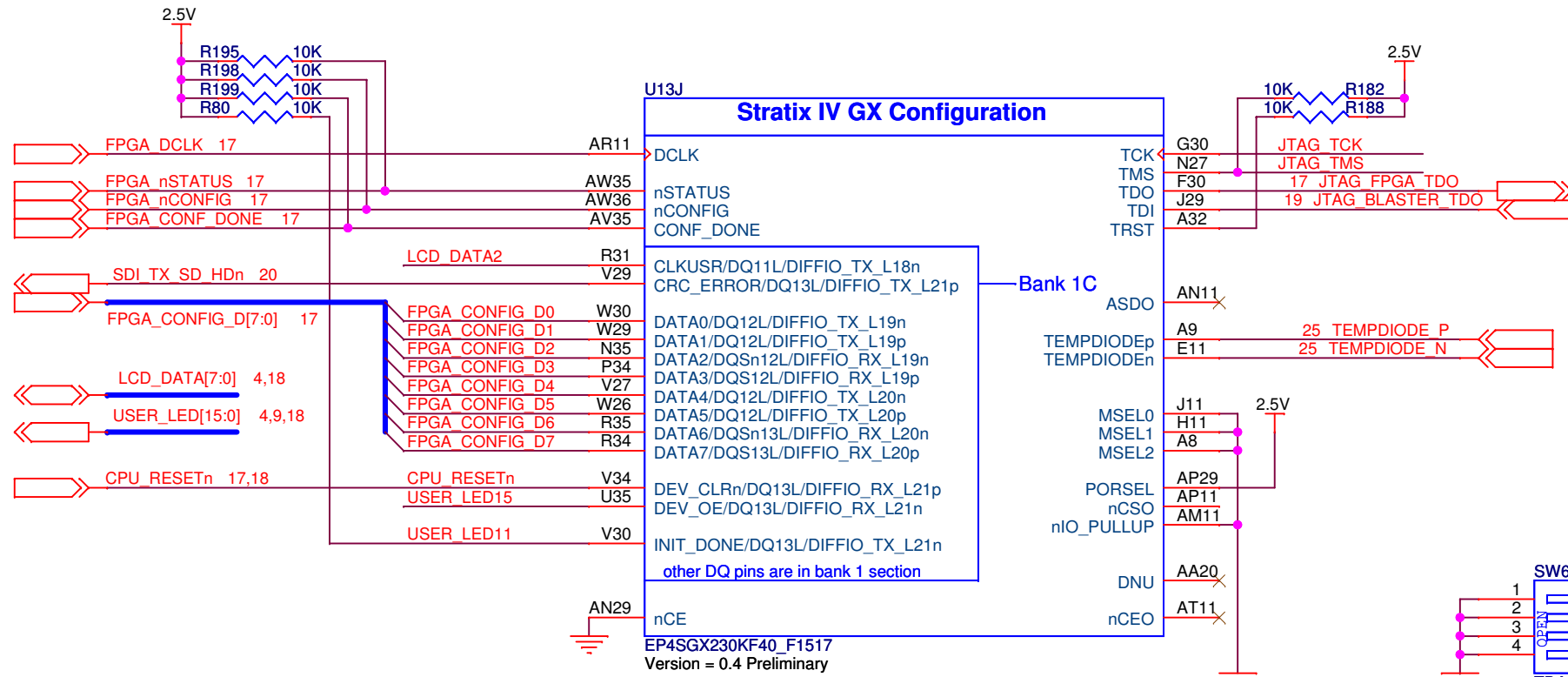
DDR3 INTERFACE



QDR II & USER I/O INTERFACES



Stratix IV GX Configuration



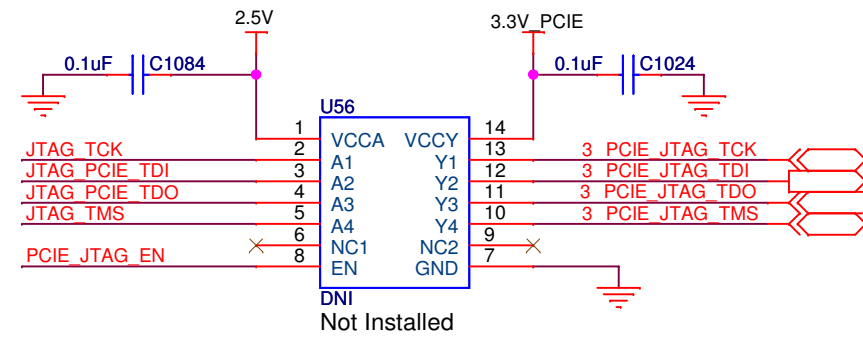
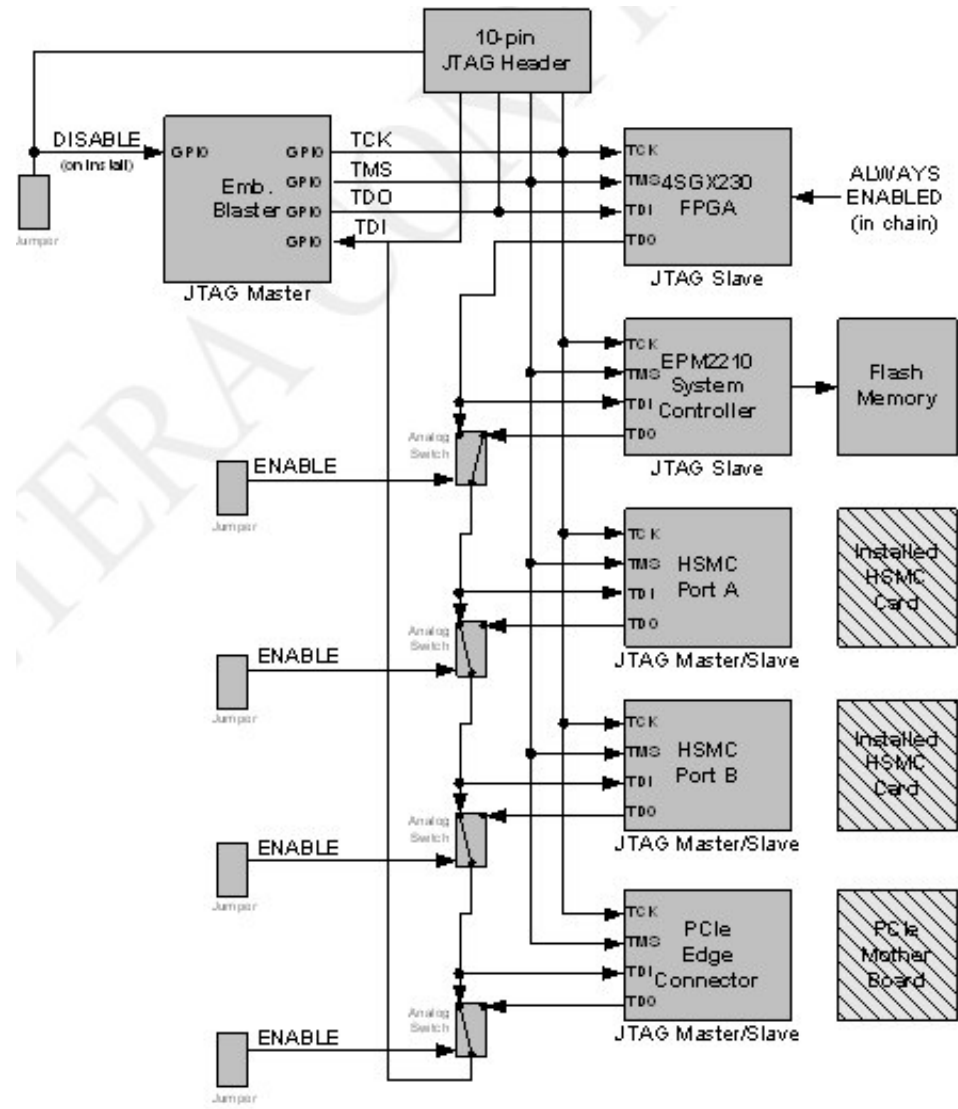
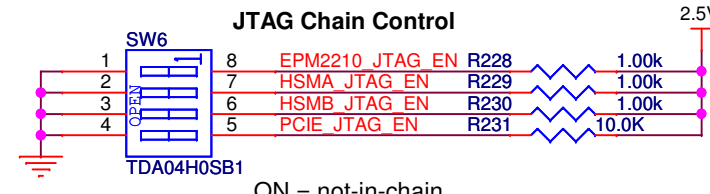
ISL54050 Switch Functions

When Pins 4 & 8 are:
 LOW --> Pins 5 & 7 = ON and Pins 2 & 10 = OFF
 HIGH --> Pins 2 & 10 = ON and Pins 5 & 7 = OFF

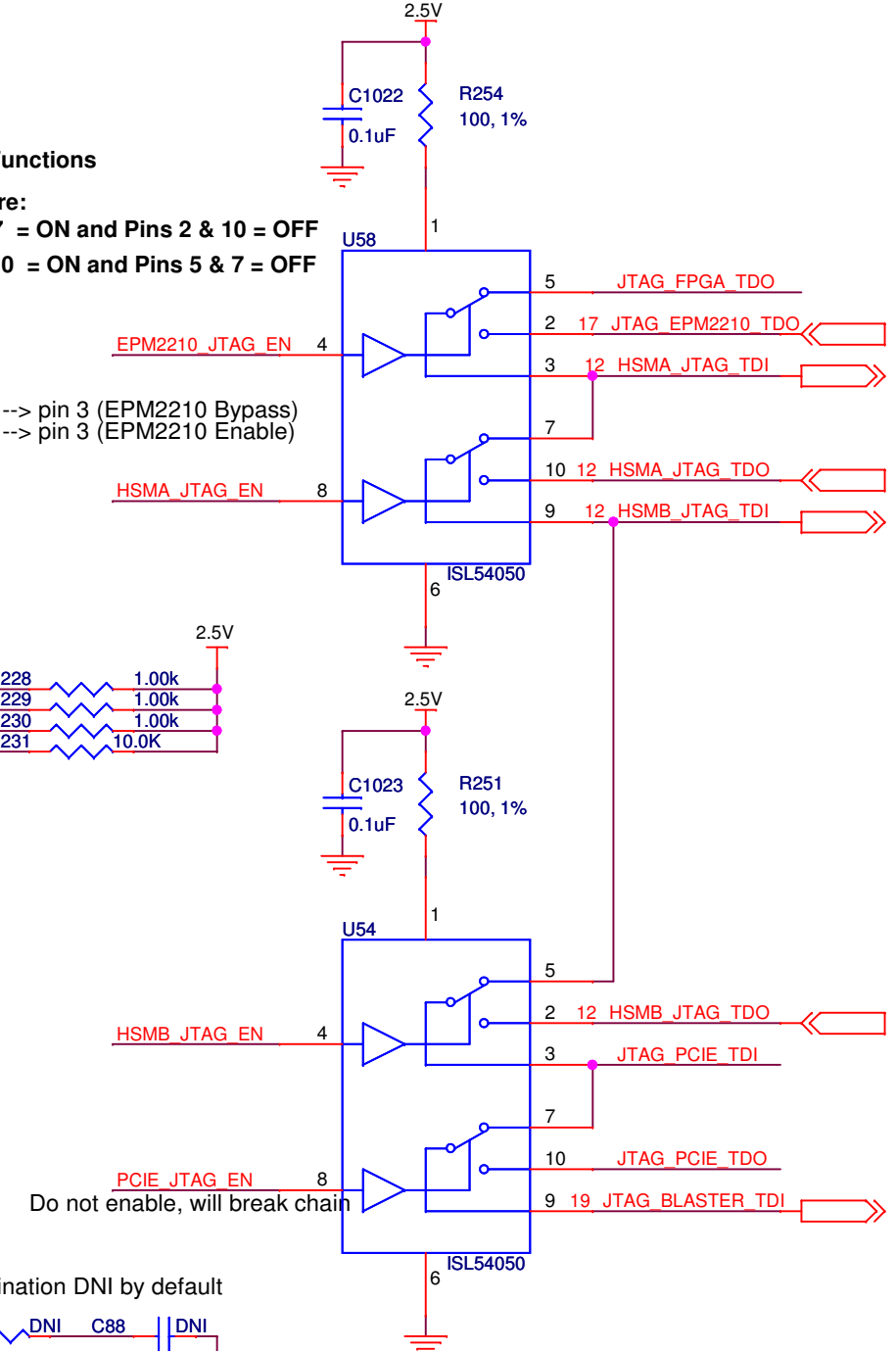
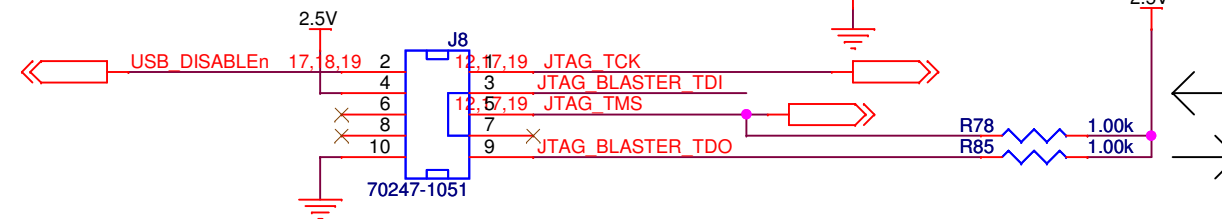
Logic 0 = pin 5 --> pin 3 (EPM2210 Bypass)
 Logic 1 = pin 2 --> pin 3 (EPM2210 Enable)

JTAG Chain Control

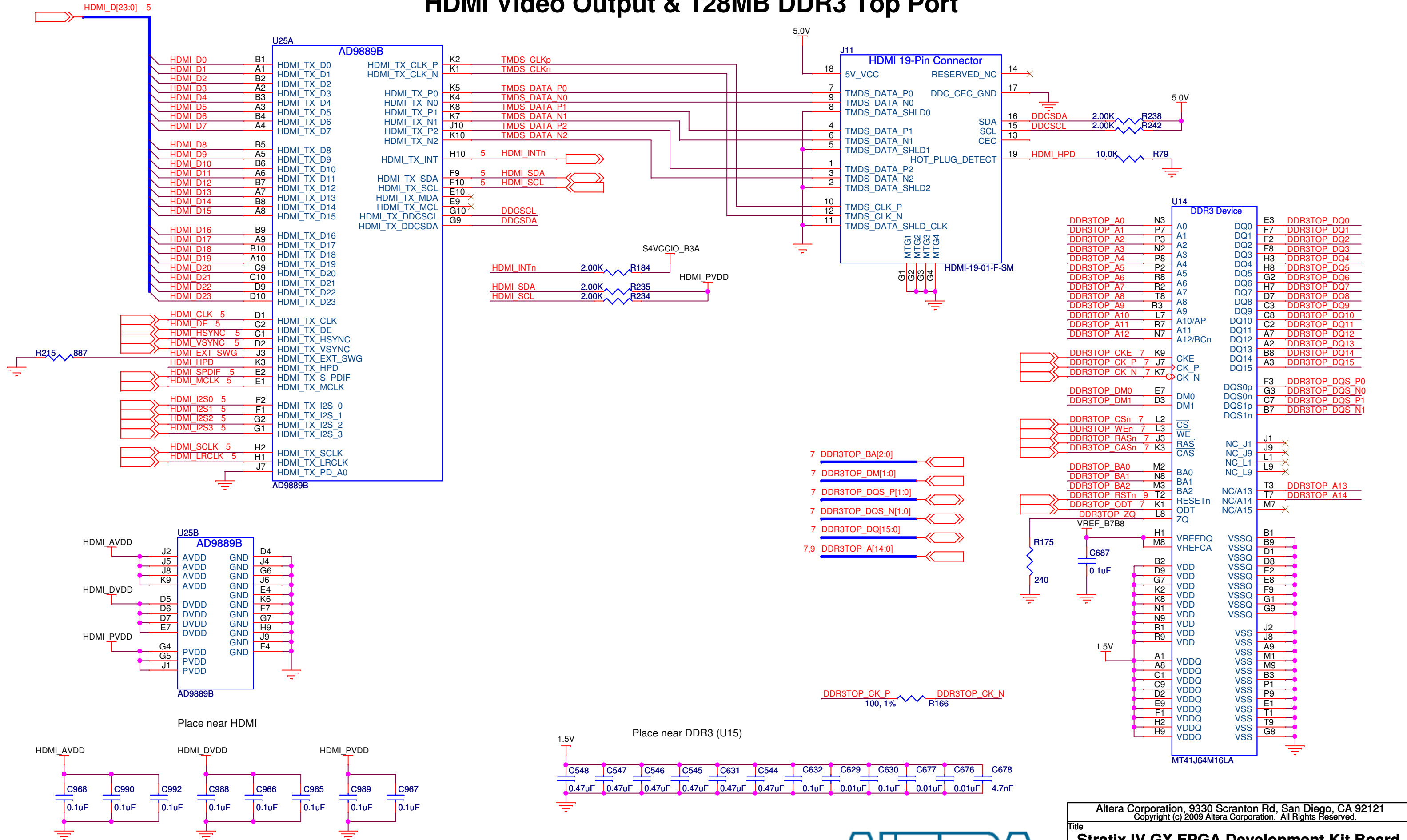
ON = not-in-chain
 OFF = in-chain



USB Blaster Programming Header (uses JTAG mode only)



HDMI Video Output & 128MB DDR3 Top Port



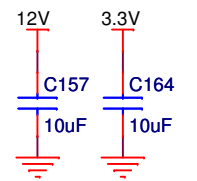
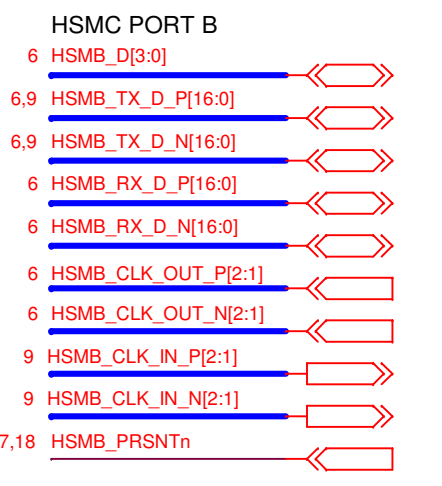
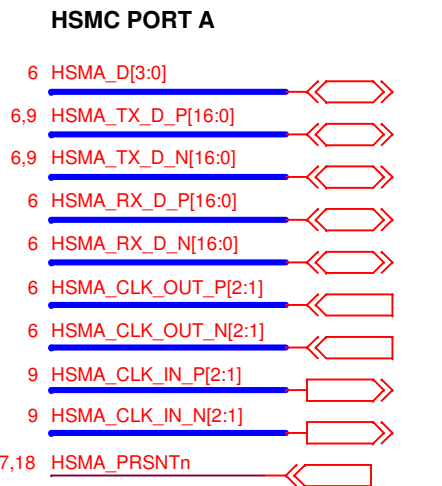
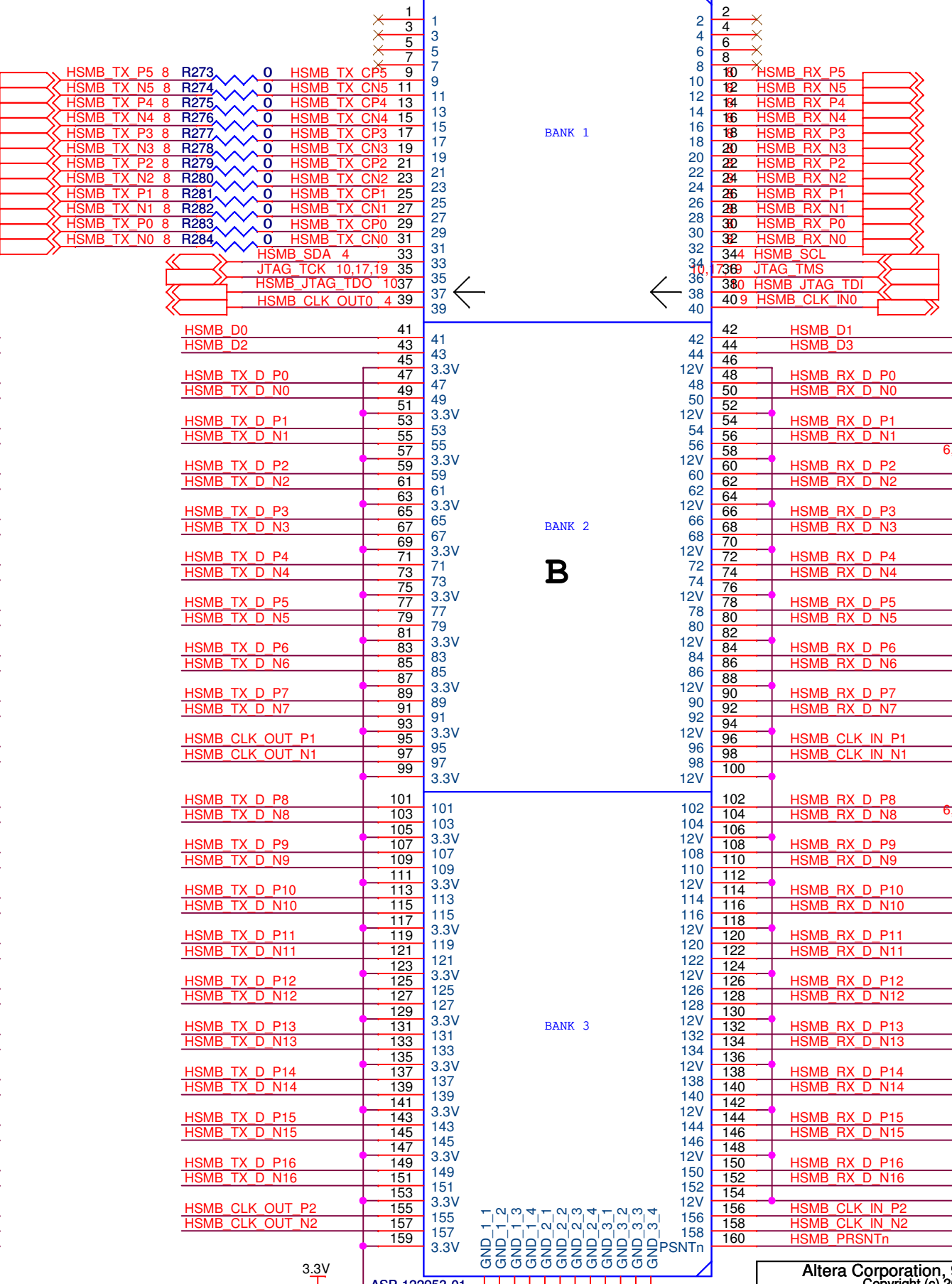
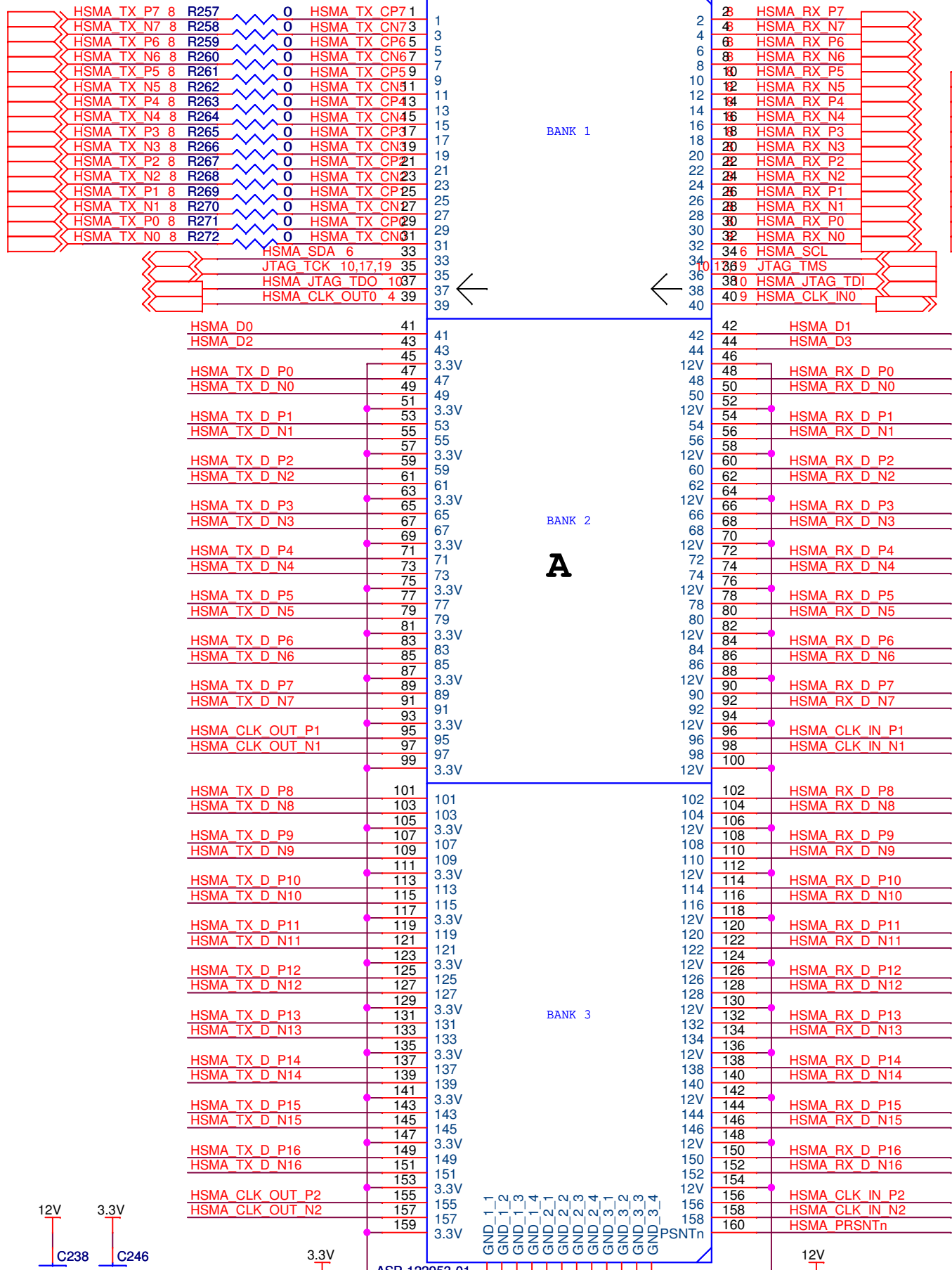
Place near HDMI

Place near DDR3 (U15)



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HSMC Port A & Port B

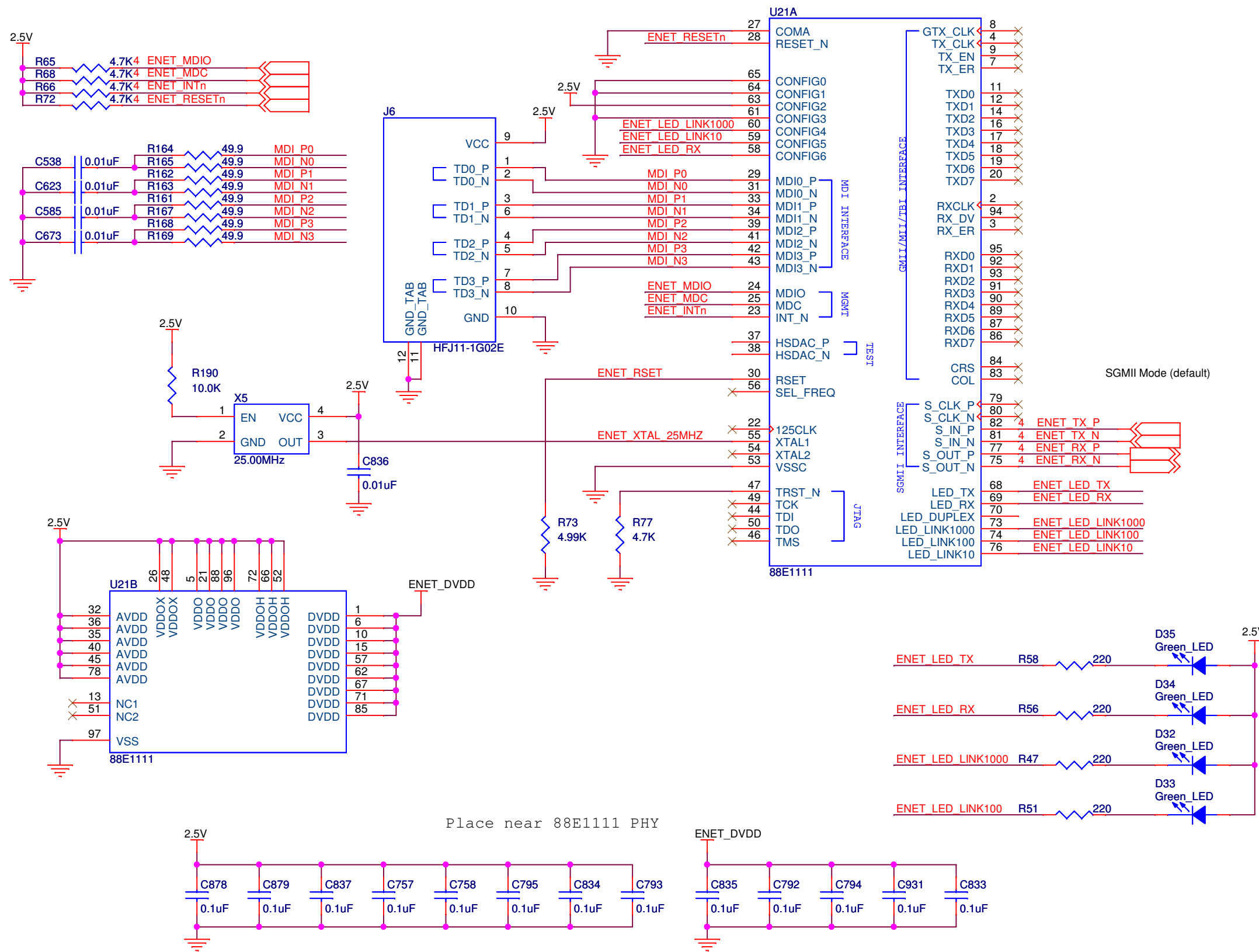


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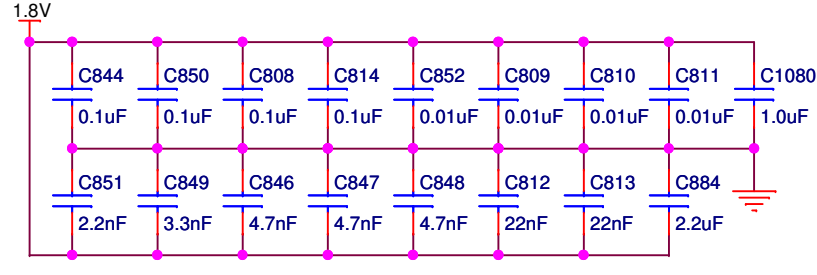
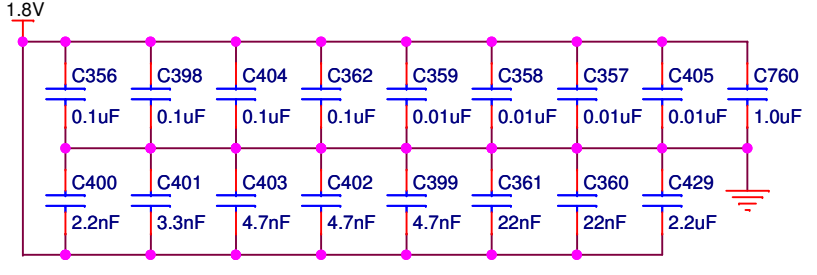
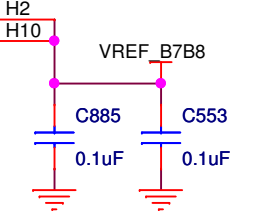
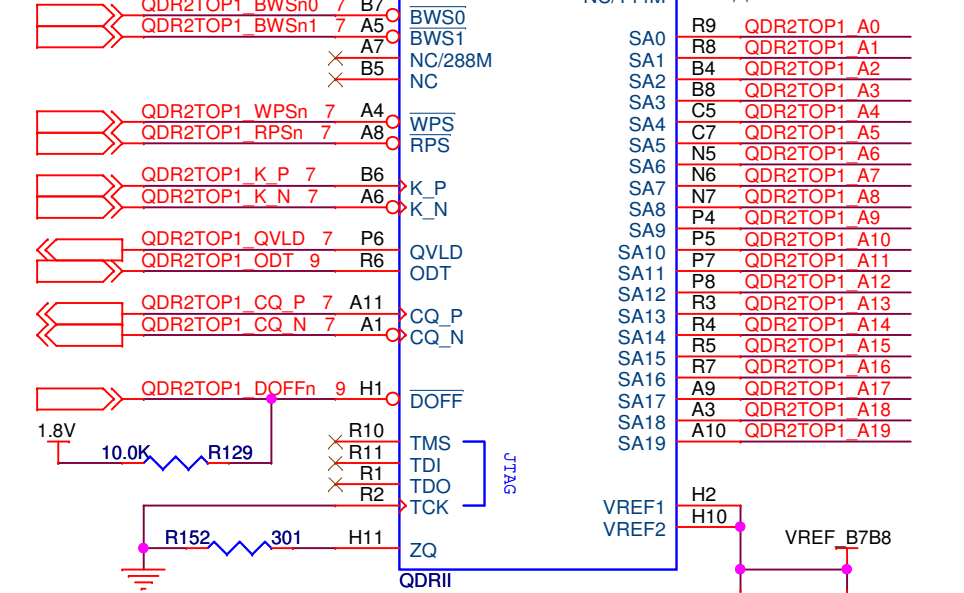
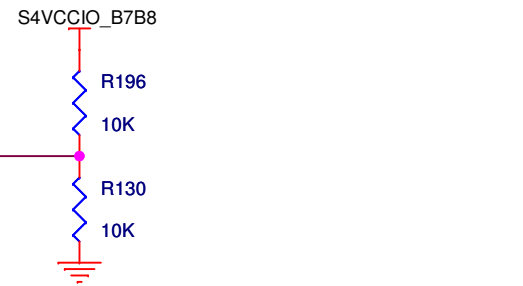
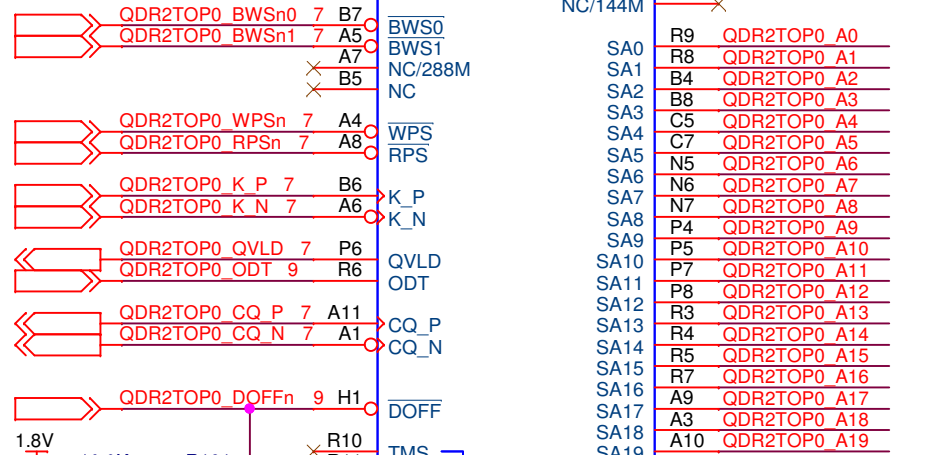
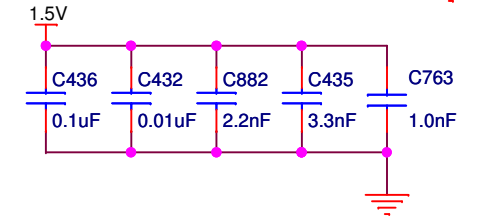
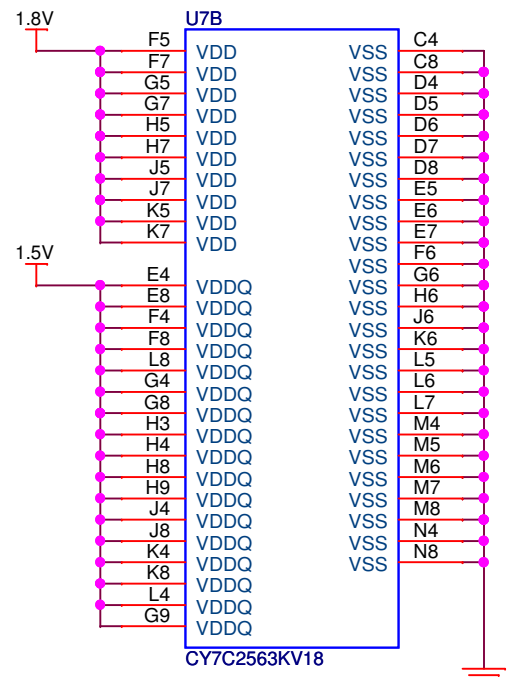
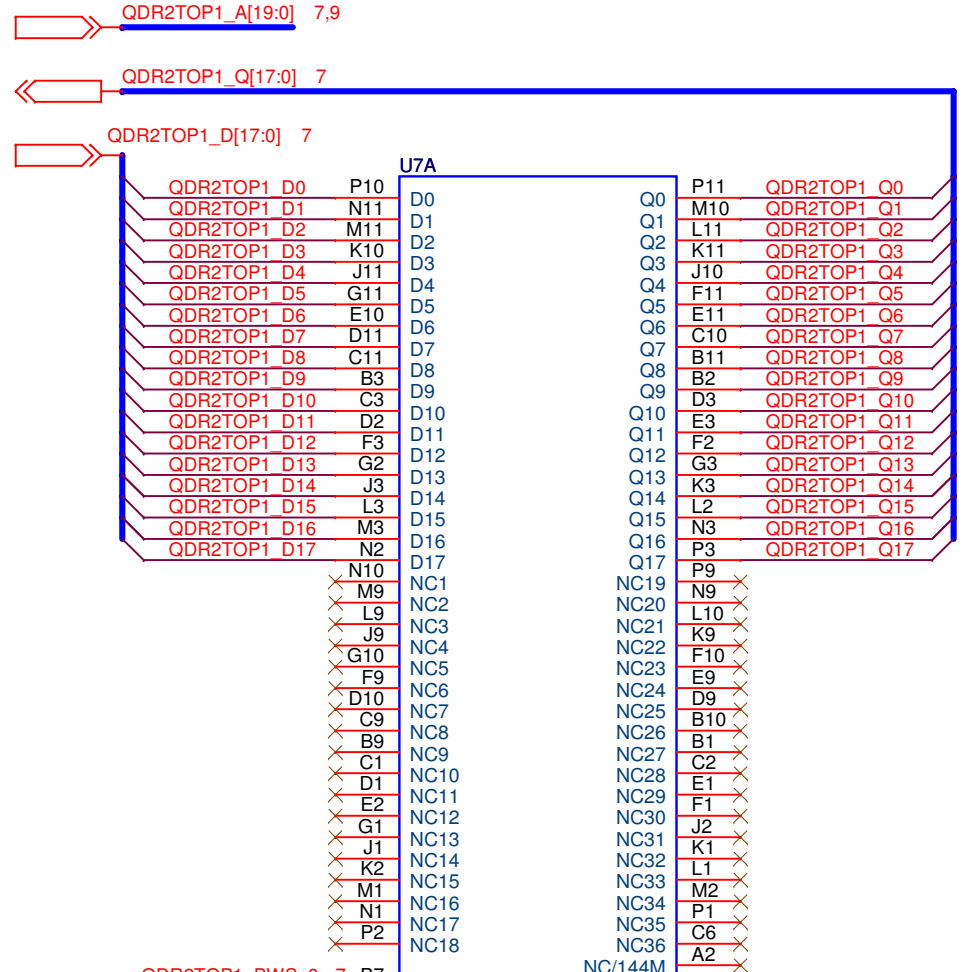
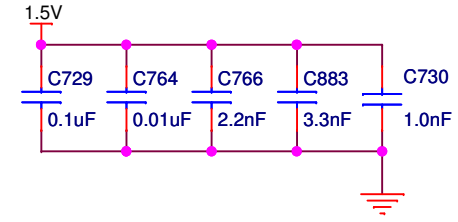
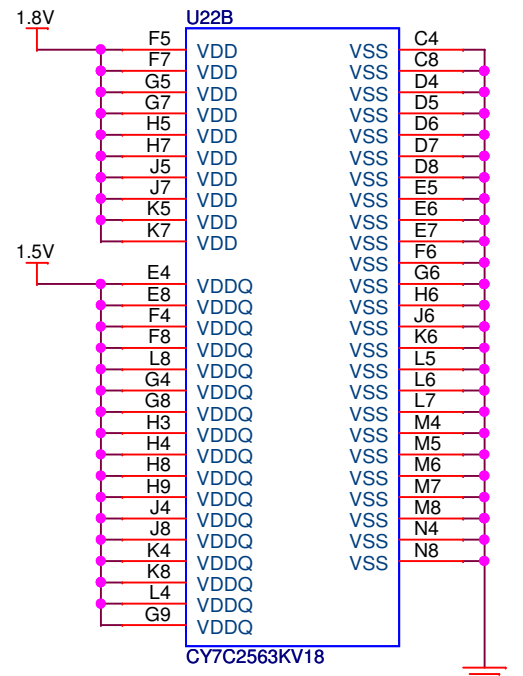
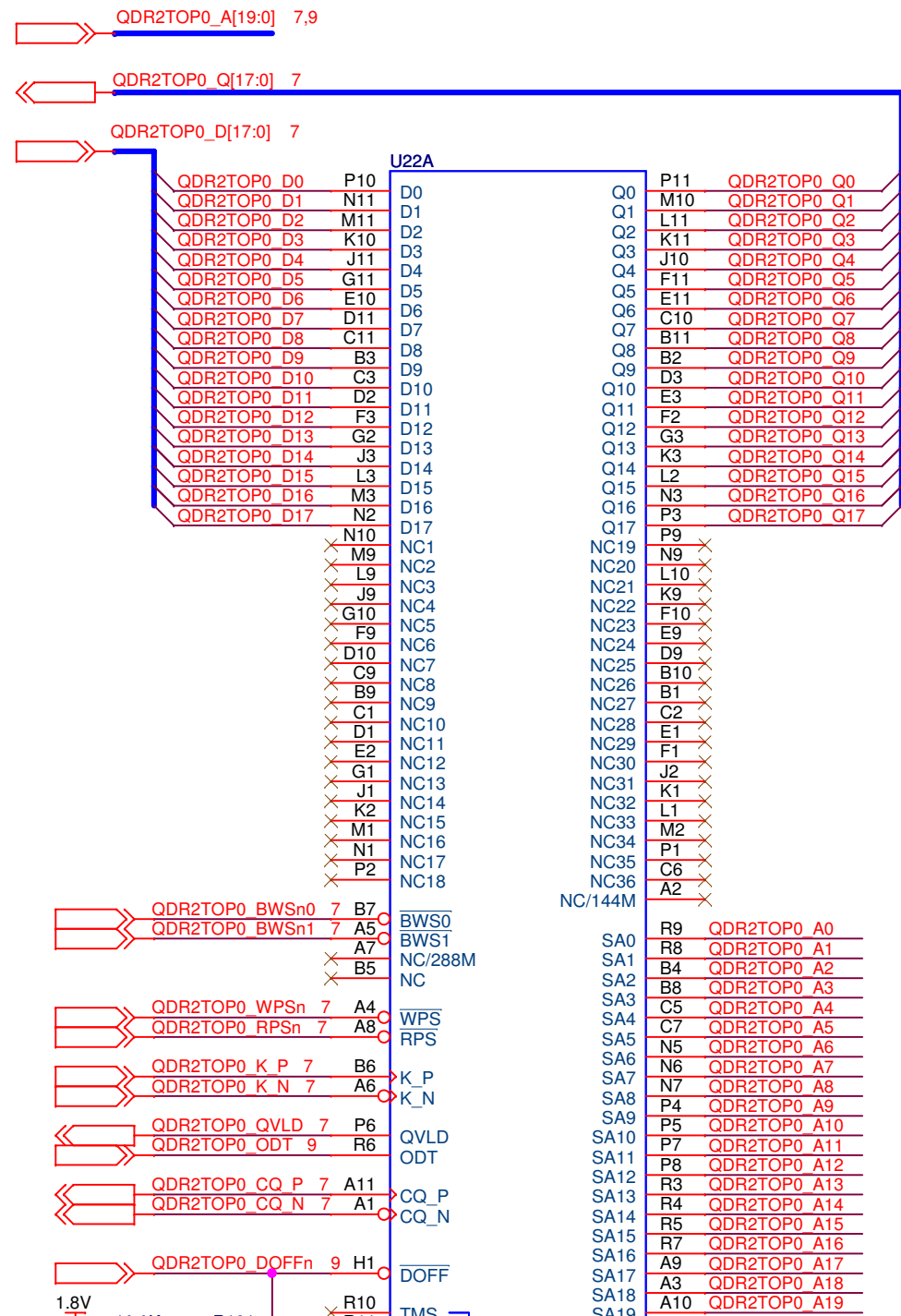
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10/100/1000 Ethernet

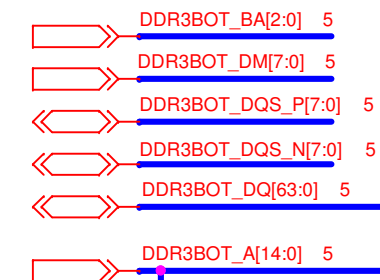
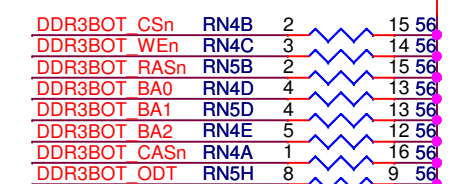
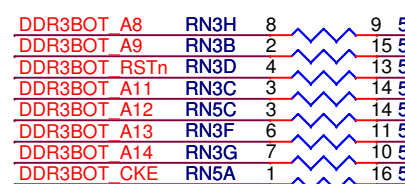
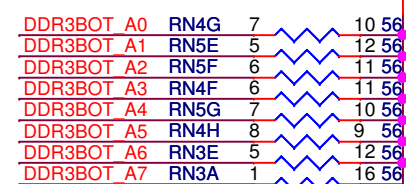
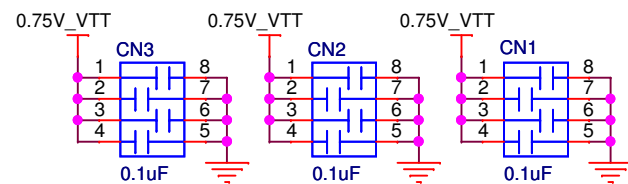


Dual 2MB QDRII+ SRAM Ports 0 & 1

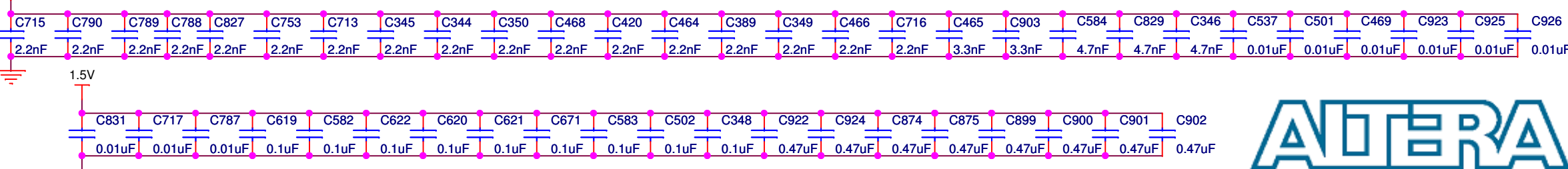
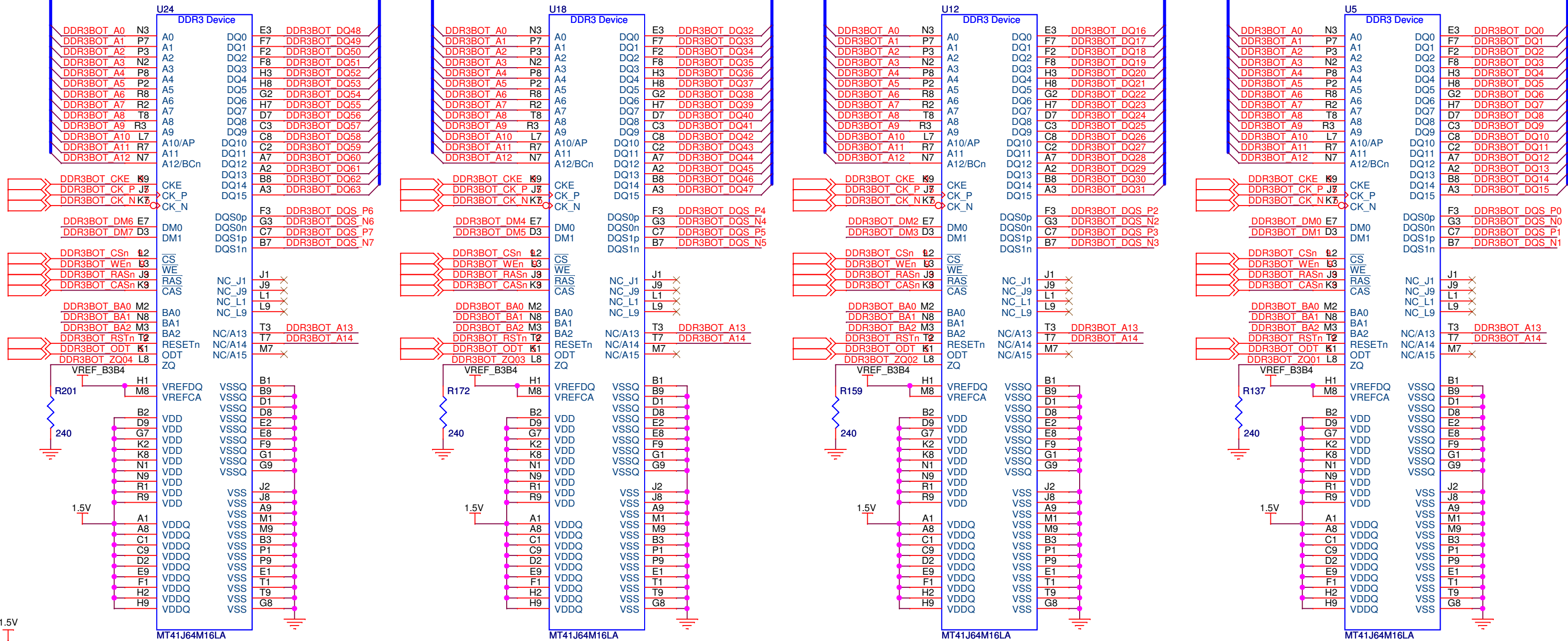


512MB DDR3 Bottom Port

DDR3BOT CK P 100, 1% R202



Note: ADDR/CMD signals daisy chain U5-->U12-->U18-->U24

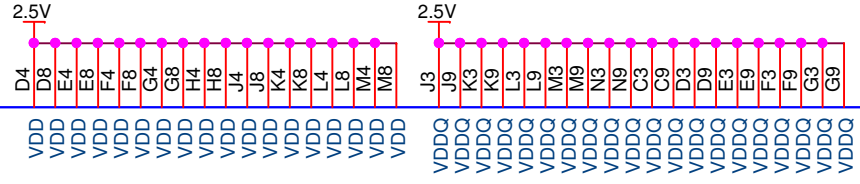


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SRAM & FLASH

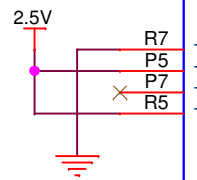
FSM BUS

FSM_D[31:0] 4,17
 FSM_A[25:0] 4,17
 SRAM_BWn[3:0] 4



FSM A2 R6 A0
 FSM A3 P6 A1
 FSM A4 A2 A2
 FSM A5 A10 A3
 FSM A6 B2 A4
 FSM A7 B10 A4
 FSM A8 N6 A5
 FSM A9 P3 A6
 FSM A10 P4 A7
 FSM A11 P8 A8
 FSM A12 P9 A9
 FSM A13 P10 A10
 FSM A14 P11 A11
 FSM A15 R3 A12
 FSM A16 R4 A13
 FSM A17 R8 A14
 FSM A18 R9 A15
 FSM A19 R10 A16
 FSM A20 R11 A17
 FSM A21 B1 A18
 FSM A22 A1 NC_144M
 FSM A23 B11 NC_288M
 FSM A24 C10 NC_576M
 FSM A25 P2 NC_1G
 R2 NC_A
 NC_B

SRAM CLK 4 B6 CLK
 SRAM OEn 4 B8 OE_n
 SRAM CEn 4 A3 CE1_n
 SRAM CE2 B3 CE2
 SRAM CE3n A6 CE3_n
 SRAM MODE 17 R1 MODE
 SRAM BWn0 B5 BWA_n
 SRAM BWn1 A5 BWB_n
 SRAM BWn2 A4 BWC_n
 SRAM BWn3 B4 BWD_n
 SRAM BWEEn 4 A7 BWE_n
 SRAM GWn 4 B7 GW_n
 SRAM ADSCn 4 A8 ADSC_n
 SRAM ADSPn 4 B9 ADSP_n
 SRAM ADVn 4 A9 ADV_n
 SRAM ZZ 4,17 H11 ZZ



J10 FSM D0
 J11 FSM D1
 K10 FSM D2
 K11 FSM D3
 L10 FSM D4
 L11 FSM D5
 M10 FSM D6
 M11 FSM D7
 D10 FSM D8
 D11 FSM D9
 E10 FSM D10
 E11 FSM D11
 F10 FSM D12
 F11 FSM D13
 G10 FSM D14
 G11 FSM D15
 D1 FSM D16
 D2 FSM D17
 E1 FSM D18
 E2 FSM D19
 F1 FSM D20
 F2 FSM D21
 G1 FSM D22
 G2 FSM D23
 J1 FSM D24
 J2 FSM D25
 K1 FSM D26
 K2 FSM D27
 L1 FSM D28
 L2 FSM D29
 M1 FSM D30
 M2 FSM D31

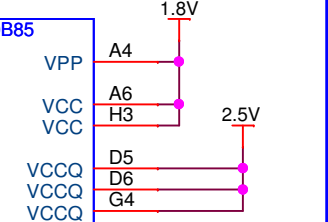
N11 4 SRAM DQP0
 C11 4 SRAM DQP1
 C1 4 SRAM DQP2
 N1 4 SRAM DQP3

A11
 C2
 H1
 P1
 H3
 H9
 H10
 N2
 N5
 N10

FLASH 512Mb (32M X 16)

U32
 PC28FxxxP30B85
 FLASH

FSM A1 A1
 FSM A2 B1 A2
 FSM A3 C1 A3
 FSM A4 D1 A4
 FSM A5 D2 A5
 FSM A6 A2 A6
 FSM A7 C2 A7
 FSM A8 A3 A8
 FSM A9 B3 A9
 FSM A10 C3 A10
 FSM A11 D3 A11
 FSM A12 C4 A12
 FSM A13 A5 A13
 FSM A14 B5 A14
 FSM A15 C5 A15
 FSM A16 D7 A16
 FSM A17 D8 A17
 FSM A18 A7 A18
 FSM A19 B7 A19
 FSM A20 C7 A20
 FSM A21 C8 A21
 FSM A22 A8 A22
 FSM A23 G1 A23
 FSM A24 H8 A24
 FSM A25 B6 A25

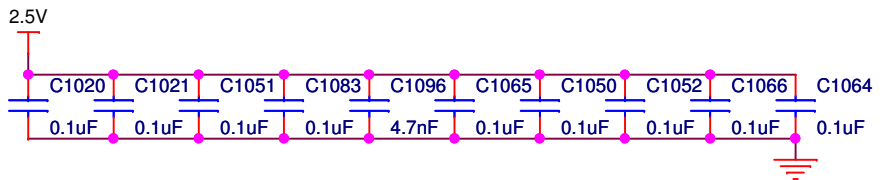
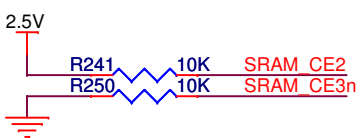
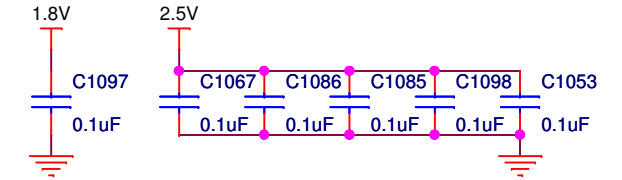
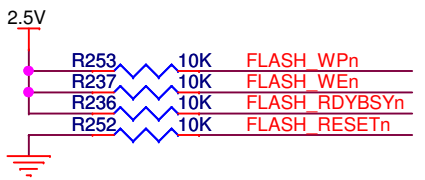


F2 FSM D0
 E2 FSM D1
 G3 FSM D2
 E4 FSM D3
 E5 FSM D4
 G5 FSM D5
 G6 FSM D6
 H7 FSM D7
 E1 FSM D8
 E3 FSM D9
 F3 FSM D10
 F4 FSM D11
 F5 FSM D12
 H5 FSM D13
 G7 FSM D14
 E7 FSM D15

FLASH CLK 4,17 E6
 FLASH RESETn 4 D4
 FLASH CEn 4,17 B4
 FLASH OEn 4,17 F8
 FLASH WEn 4,17 G8
 FLASH ADVn 4,17 F6
 FLASH WPn C6

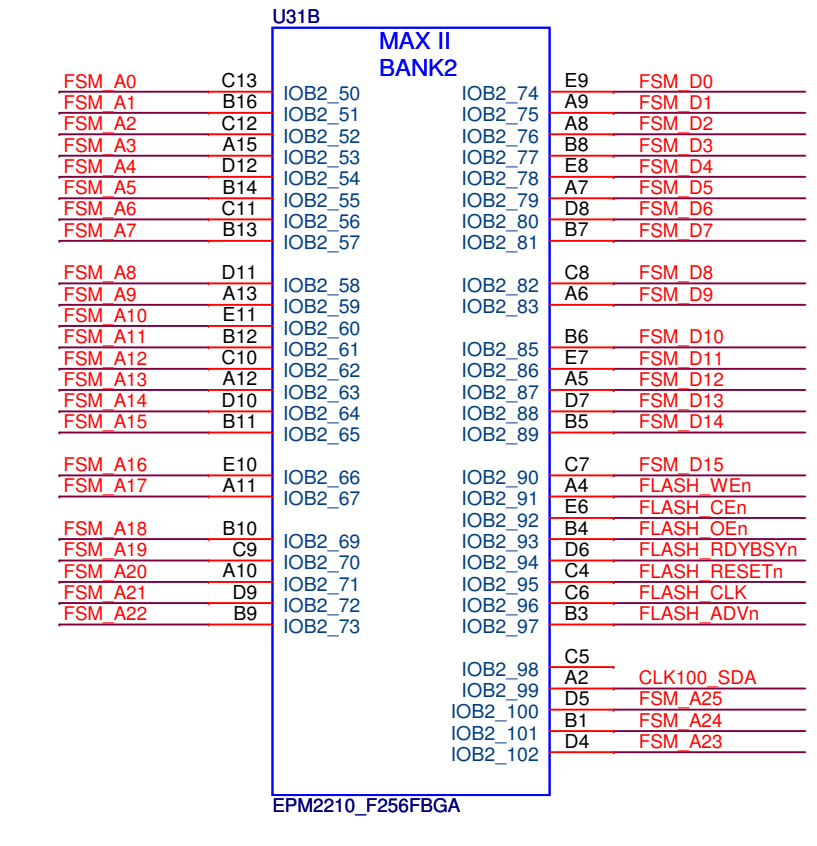
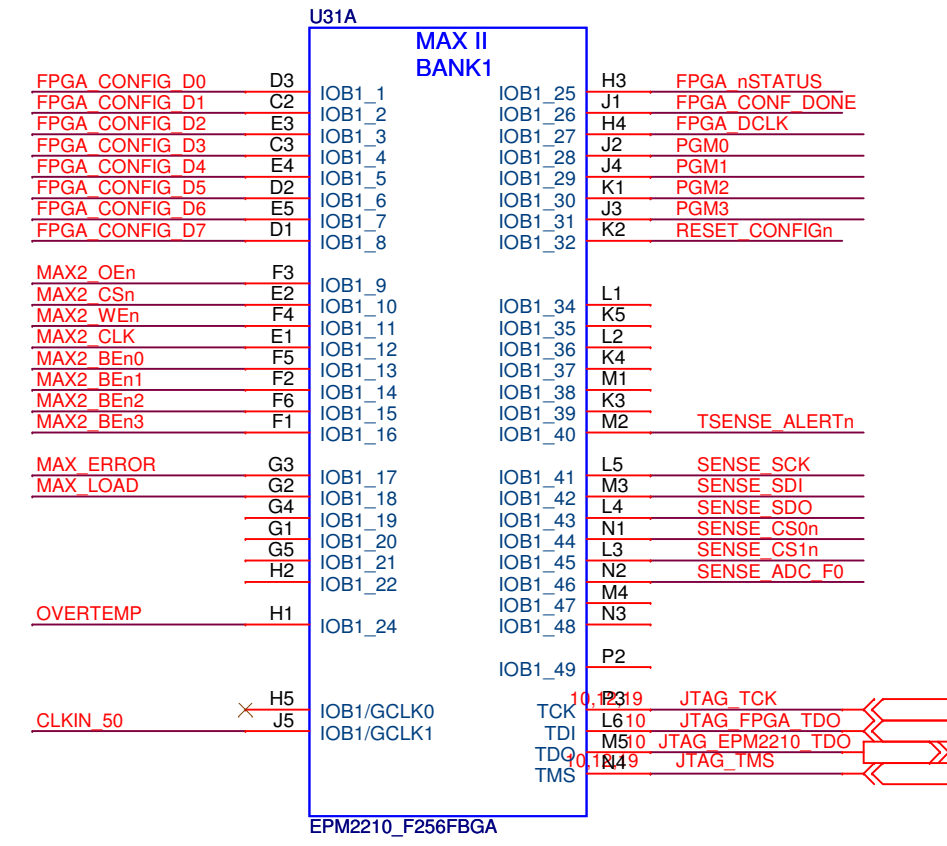
F7 4,17 FLASH RDYBSyn
 WAIT
 GND B2
 GND H2
 GND H4
 GND H6
 RFU0 H1
 RFU1 G2
 RFU2 F1
 RFU3 E8
 RFU4 B8

PC48F4400P0ZBQ0

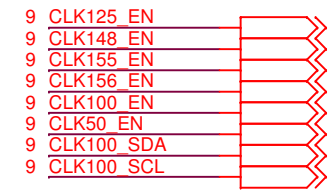


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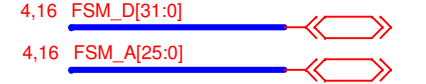
EPM2210 System Controller



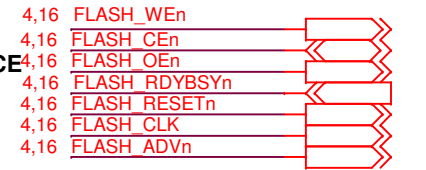
CLOCK INTERFACE



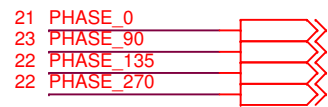
SHARED BUS



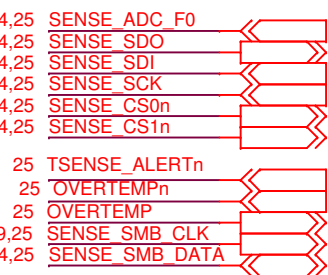
FLASH INTERFACE



REGULATOR PHASE CLOCK INTERFACE



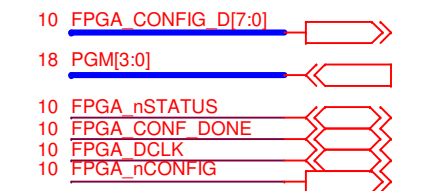
CURRENT & TEMP SENSE INTERFACES



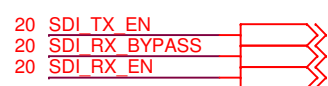
SRAM INTERFACE



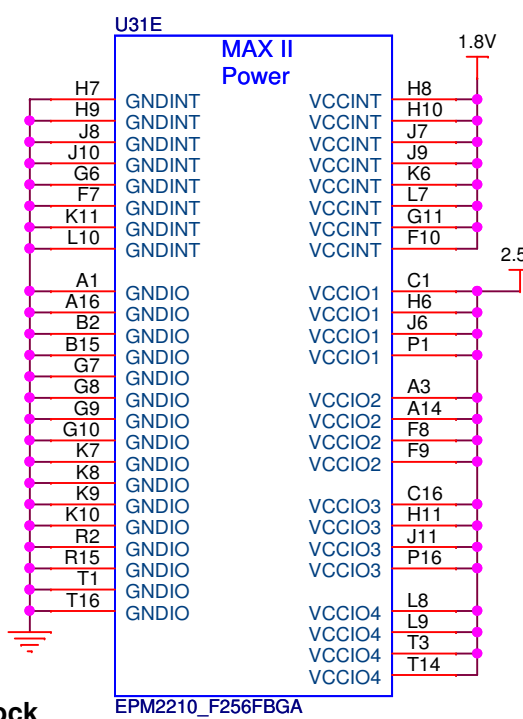
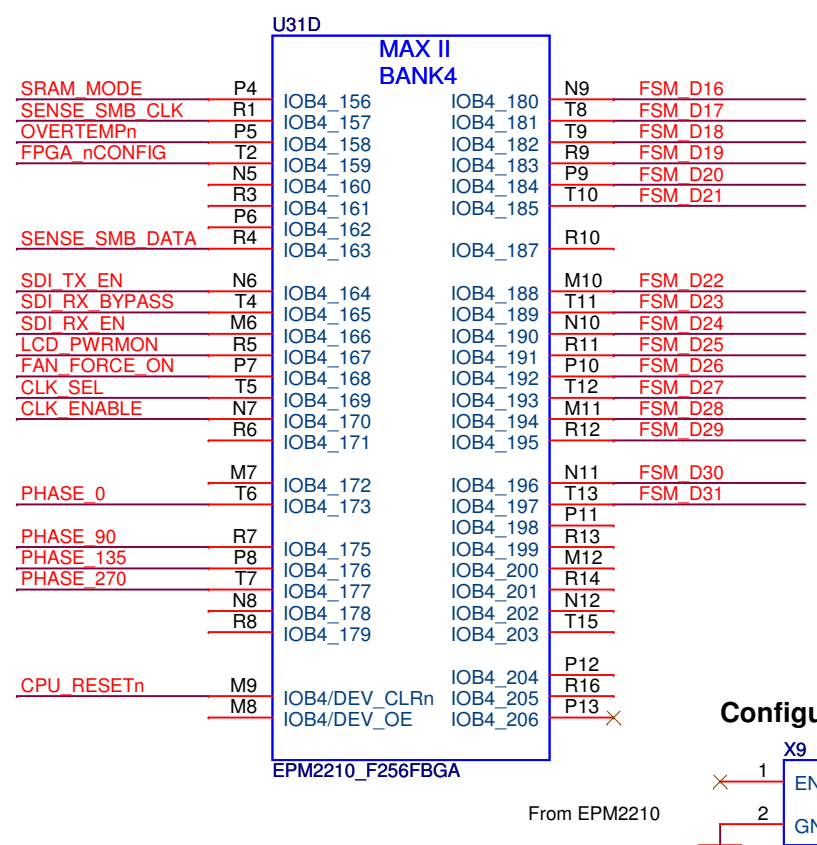
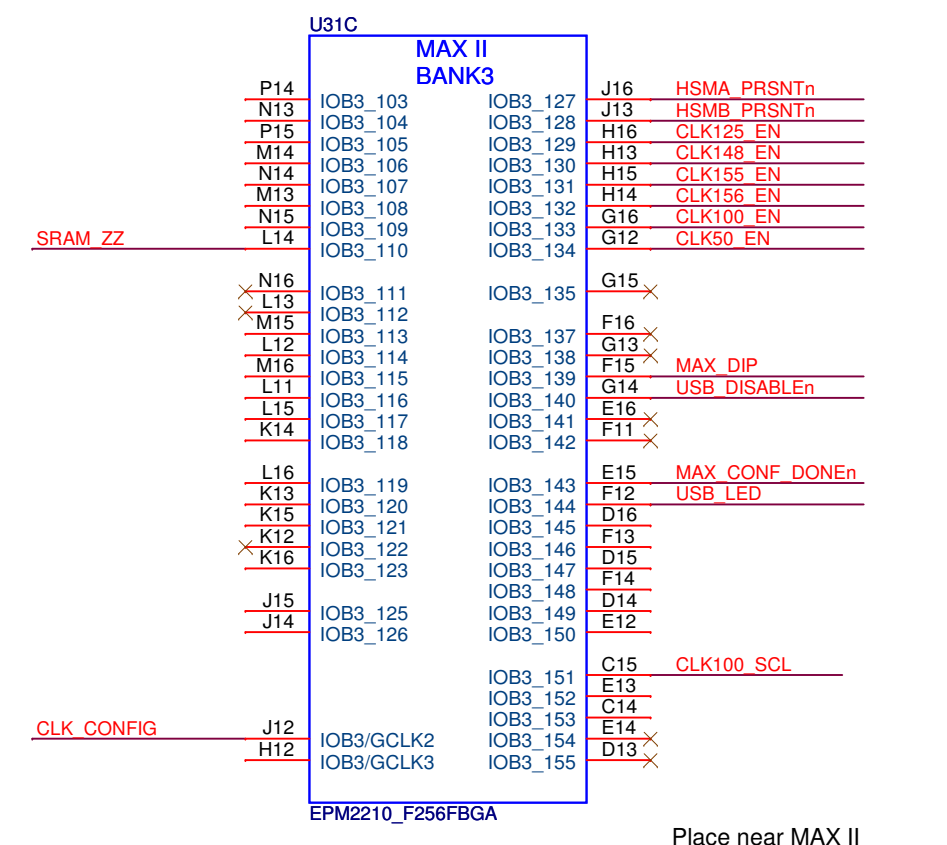
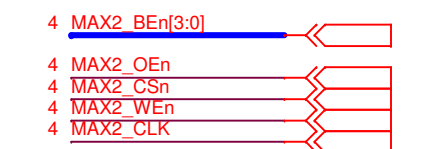
FPGA CONFIGURATION



SDI INTERFACE



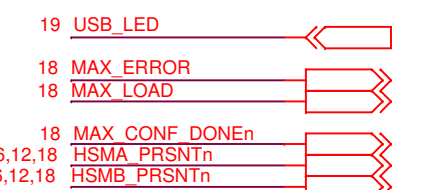
MAXII CONTROL INTERFACE



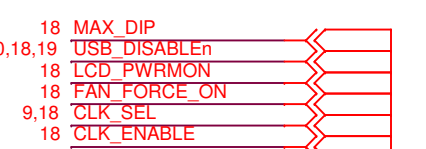
PUSH BUTTON INTERFACE



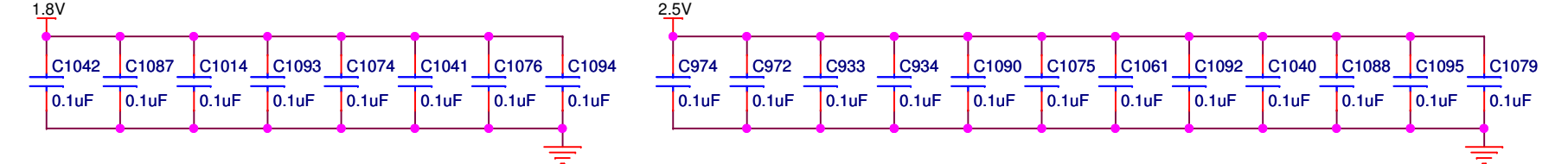
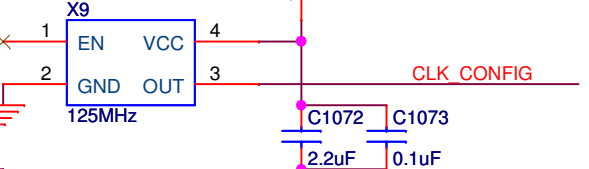
LED INTERFACE



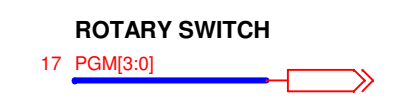
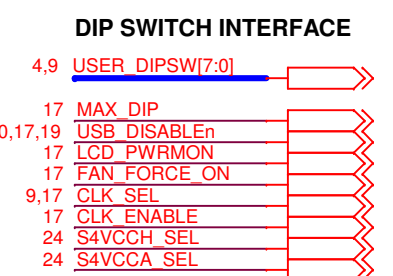
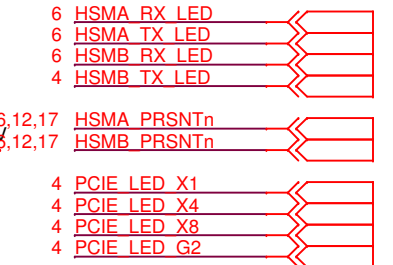
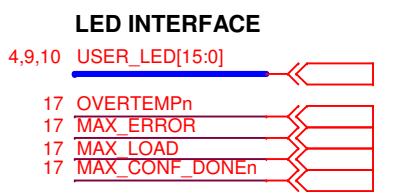
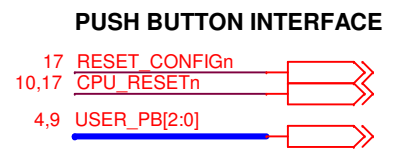
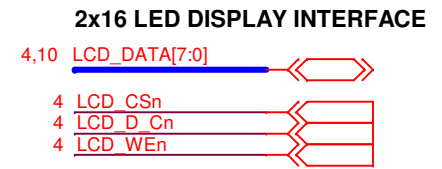
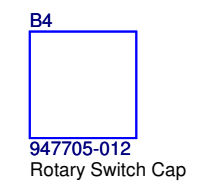
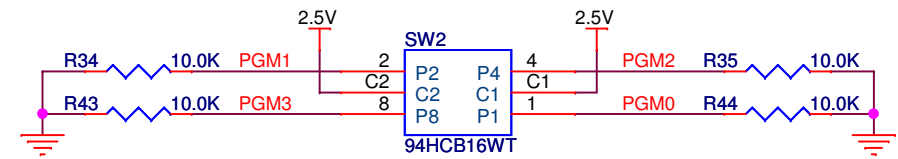
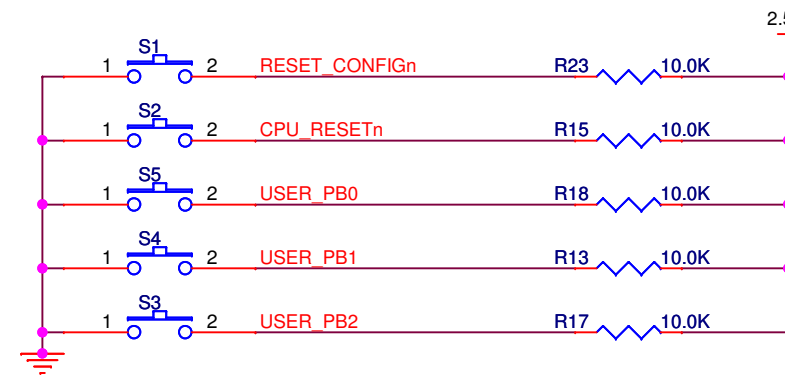
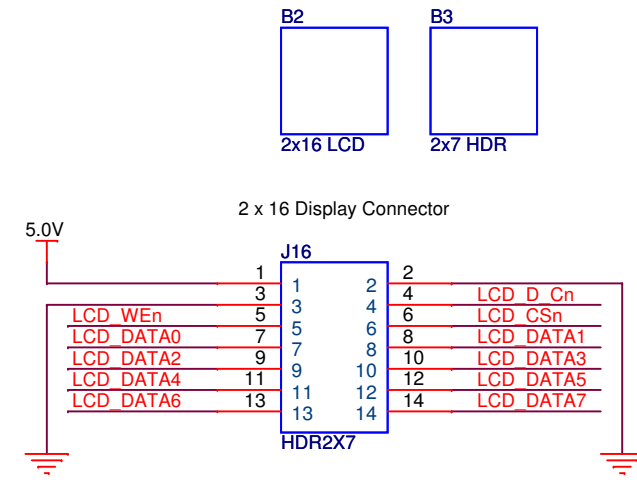
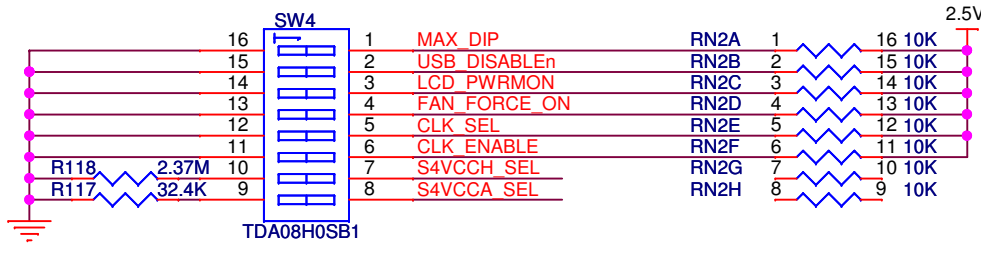
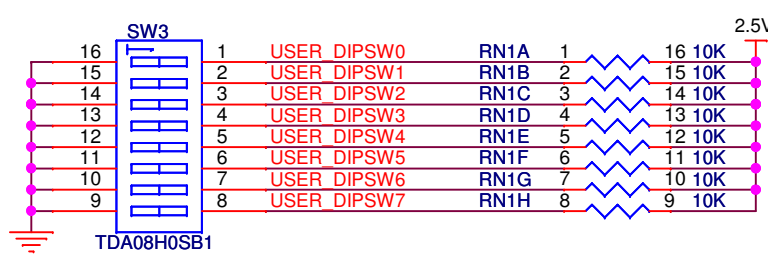
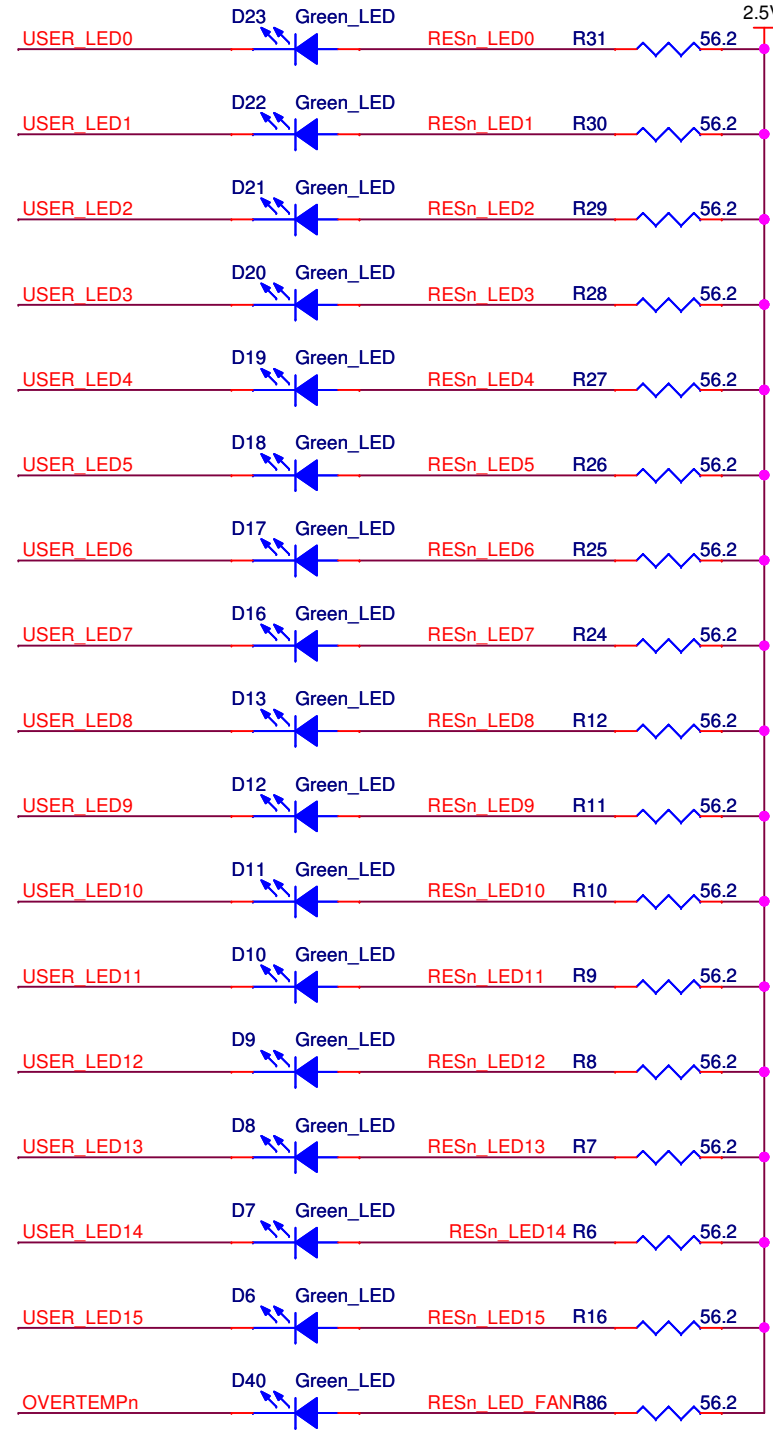
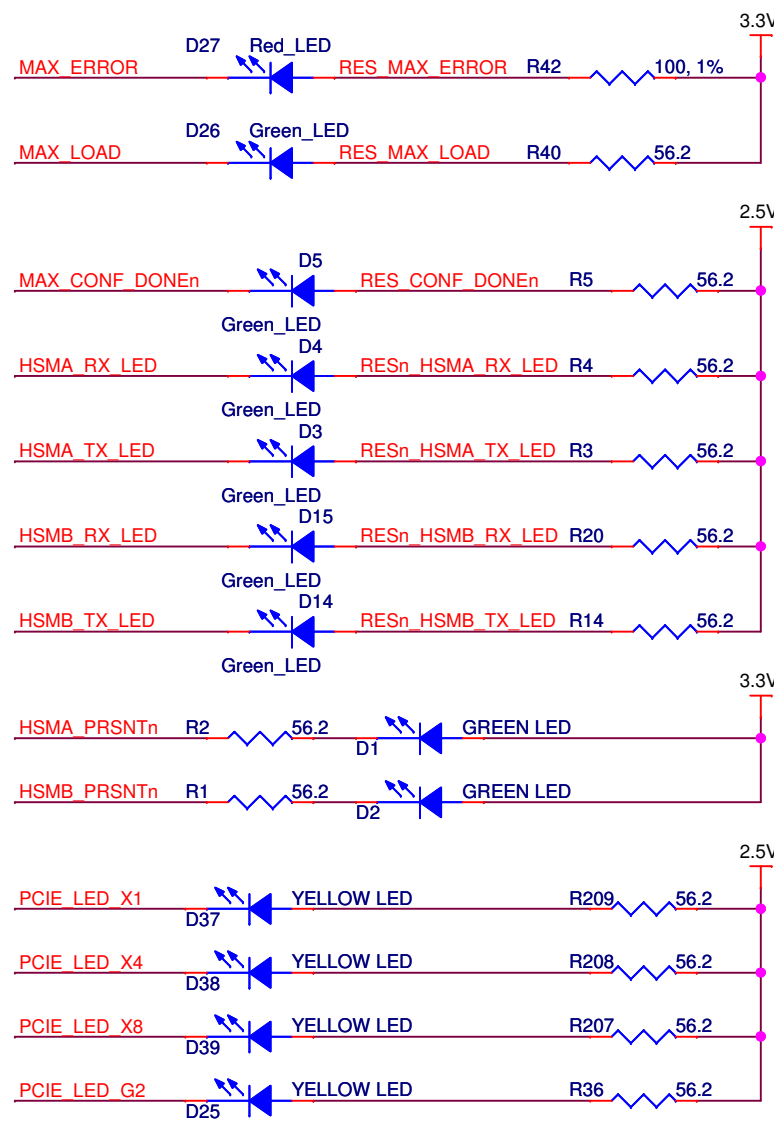
DIP SWITCH INTERFACE



Configuration Clock

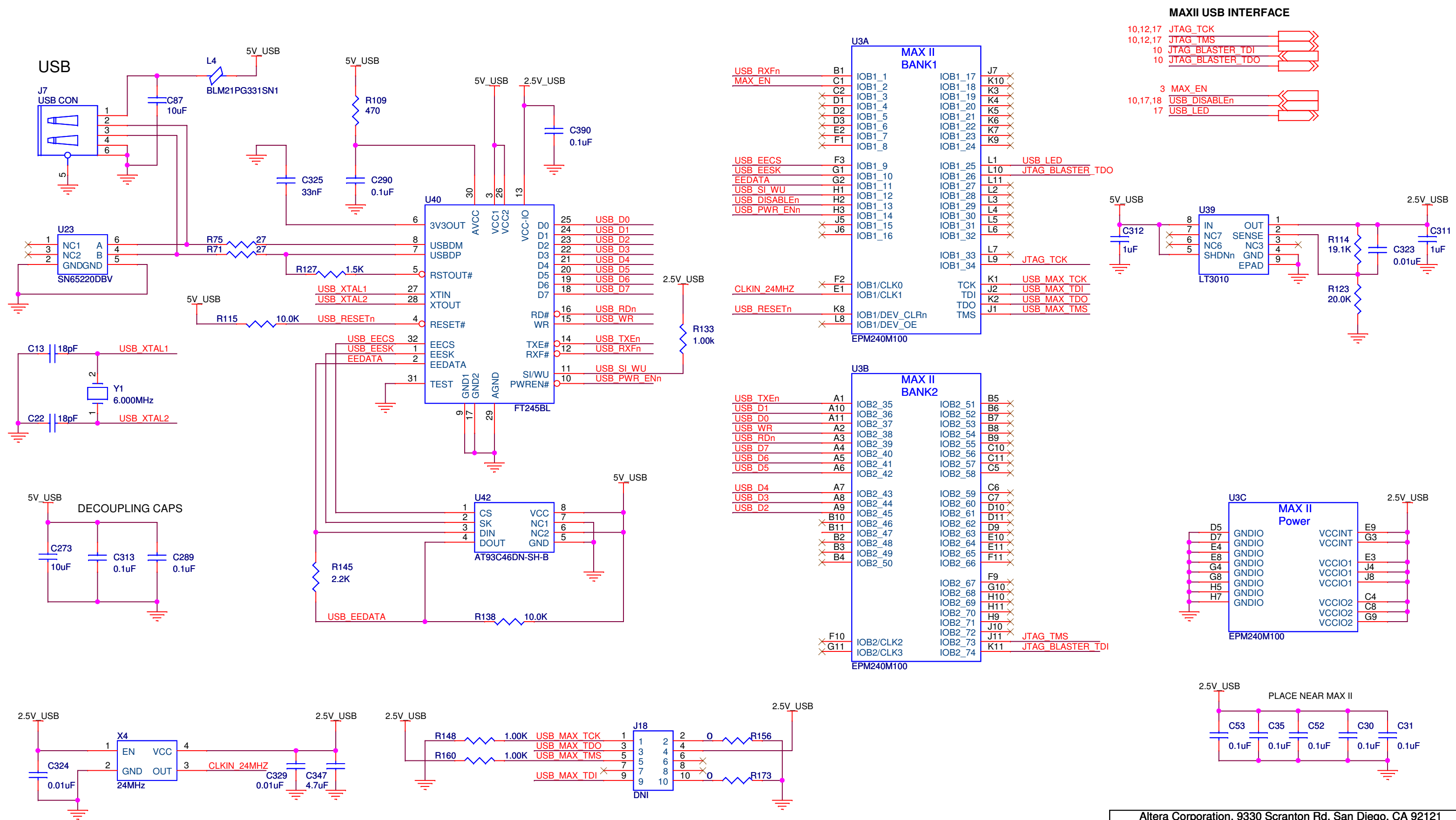


User IO & Connector

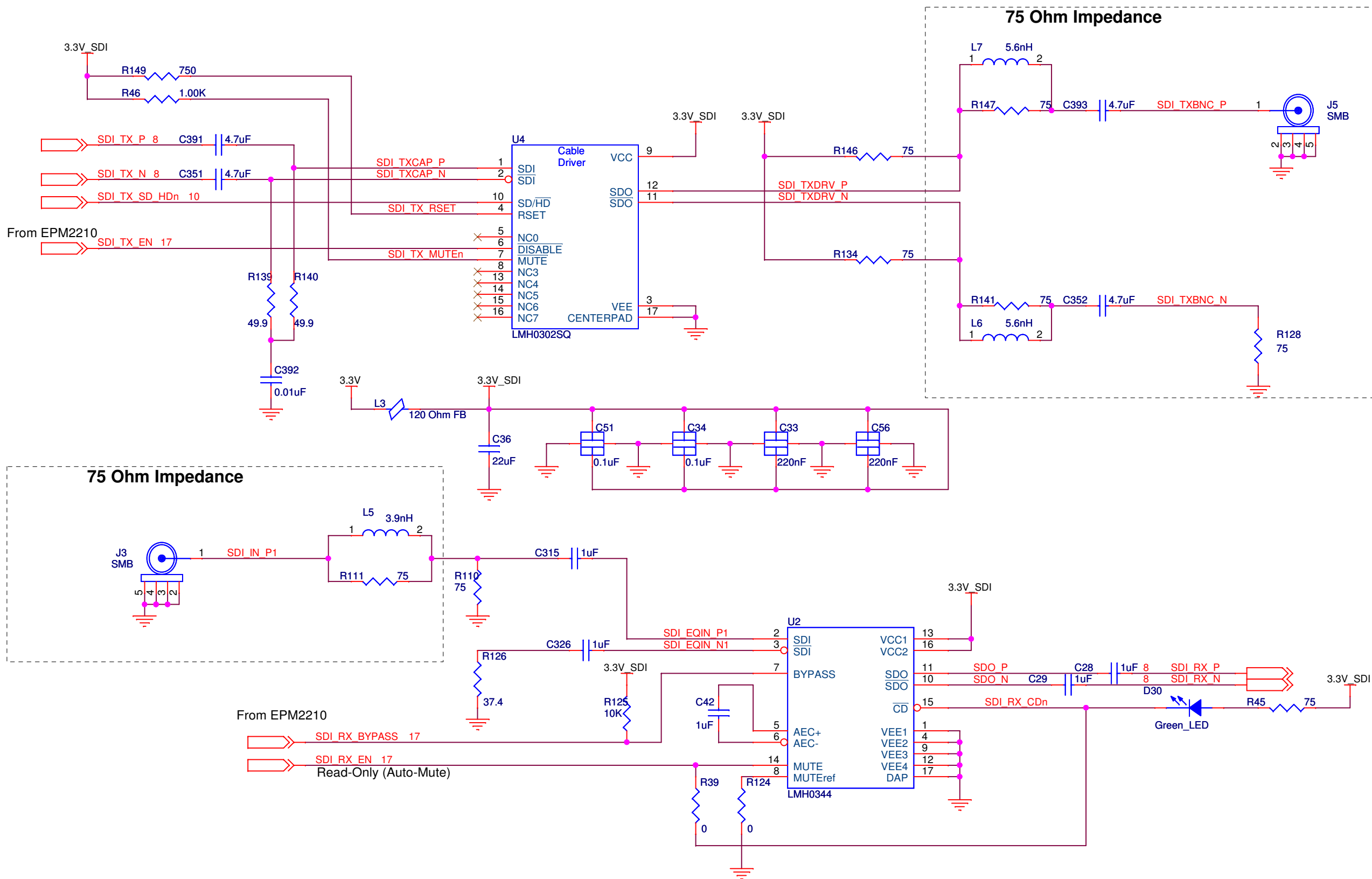


ON = 0
OFF = 1

Embedded USB Blaster

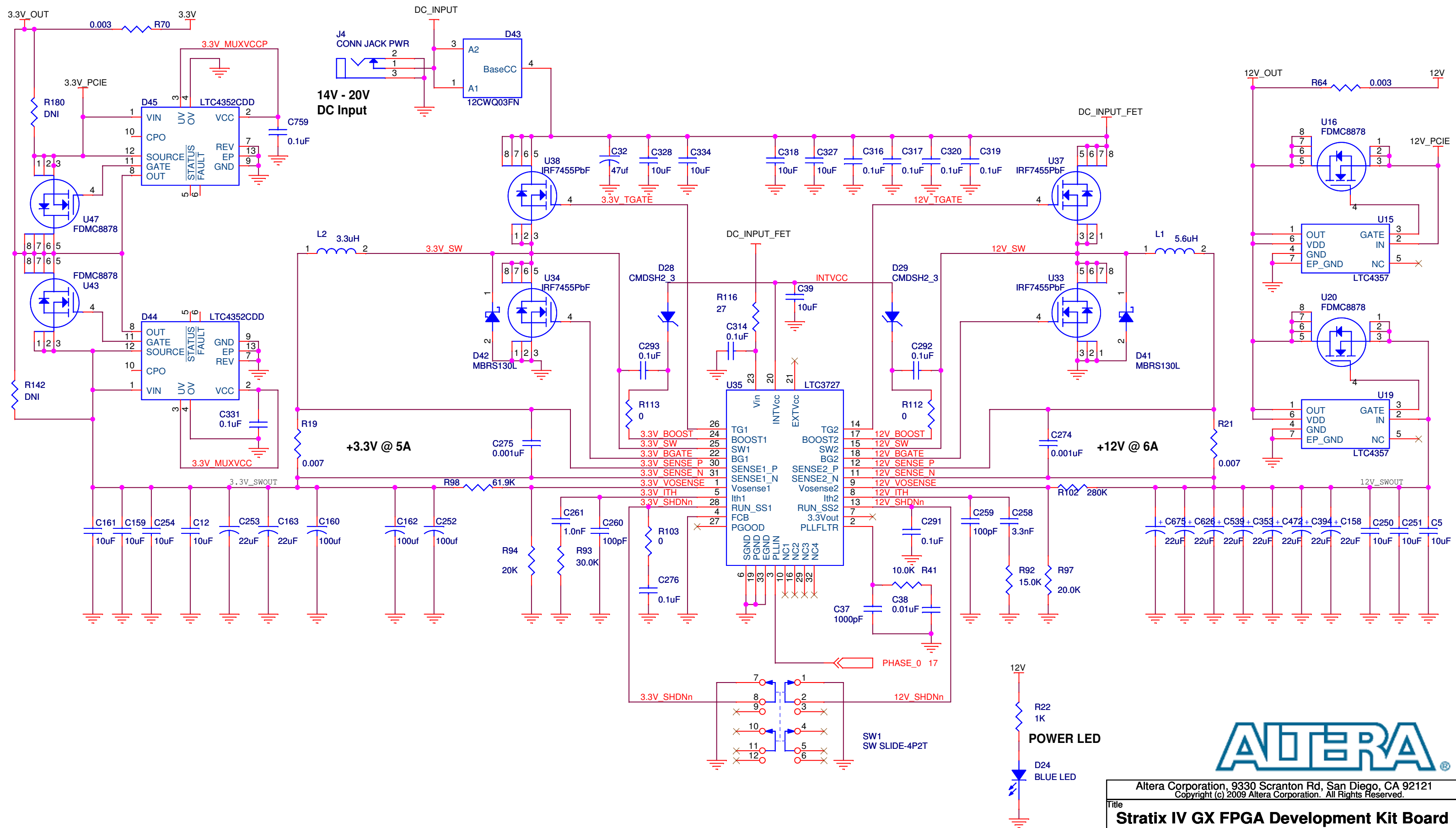


SDI Cable Driver, Equalizer, and SMB



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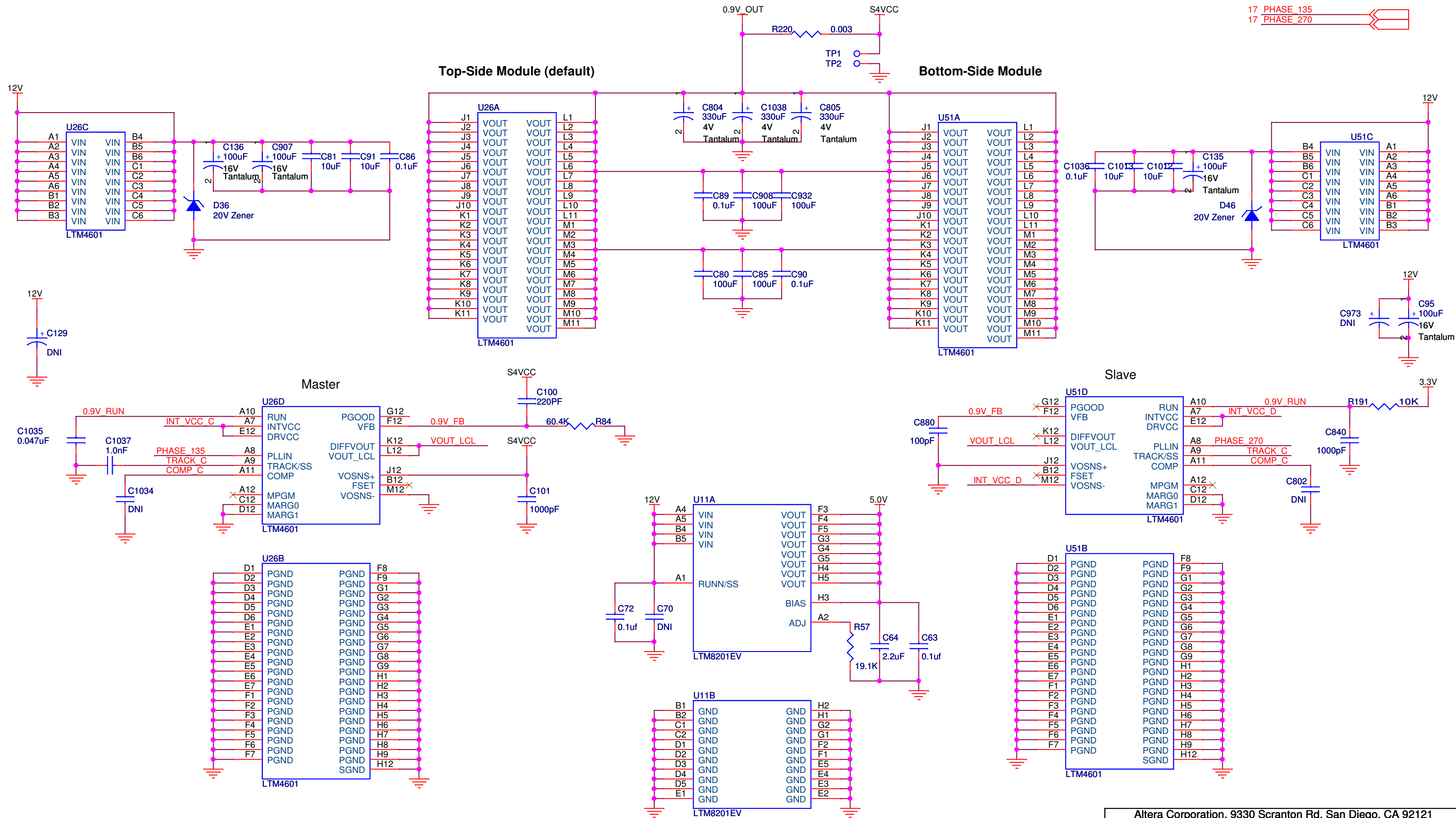
Power 1 - DC Input & 12V, 3.3V Output



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Power 2 - 0.9V & 5V



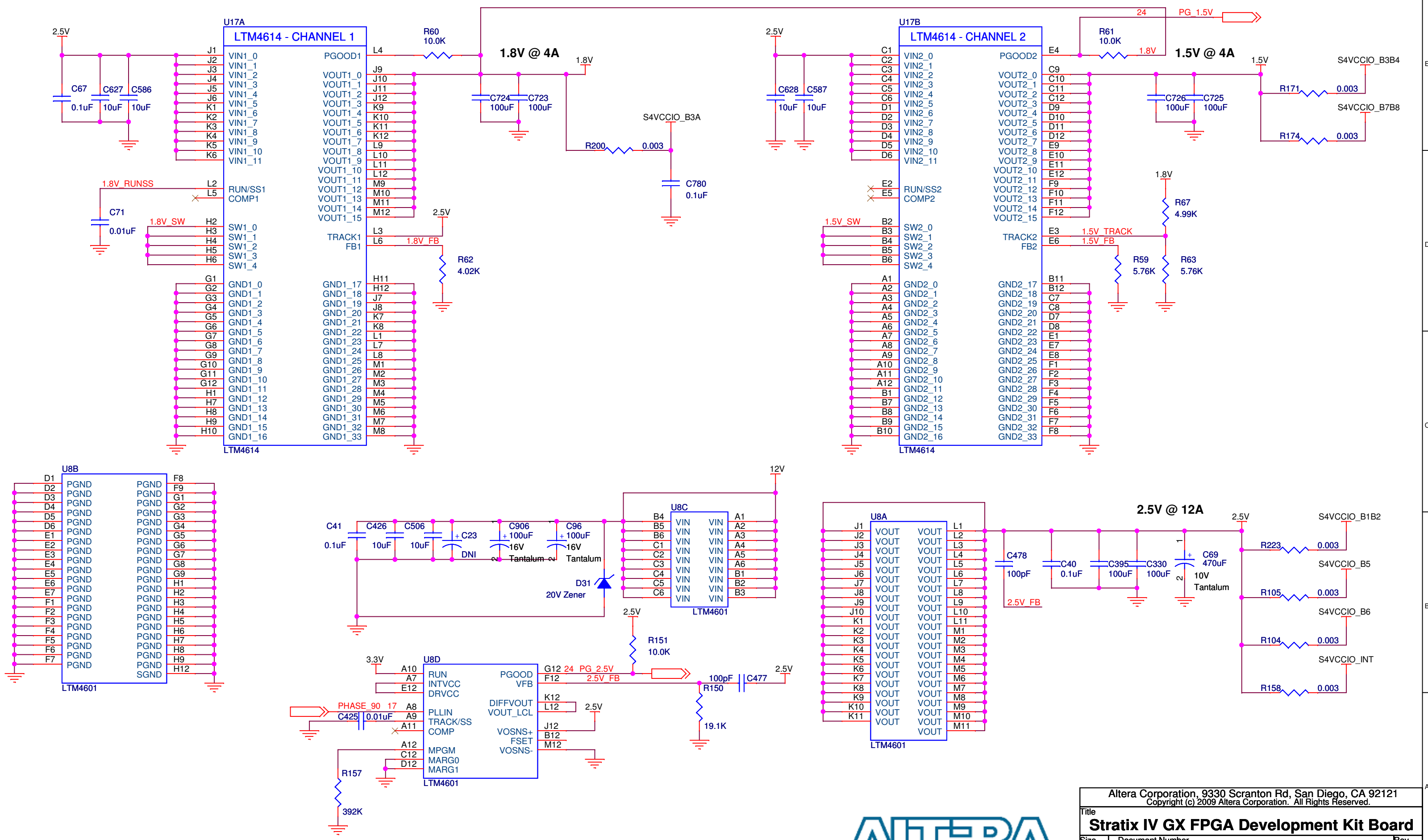
17 PHASE 135
17 PHASE 270

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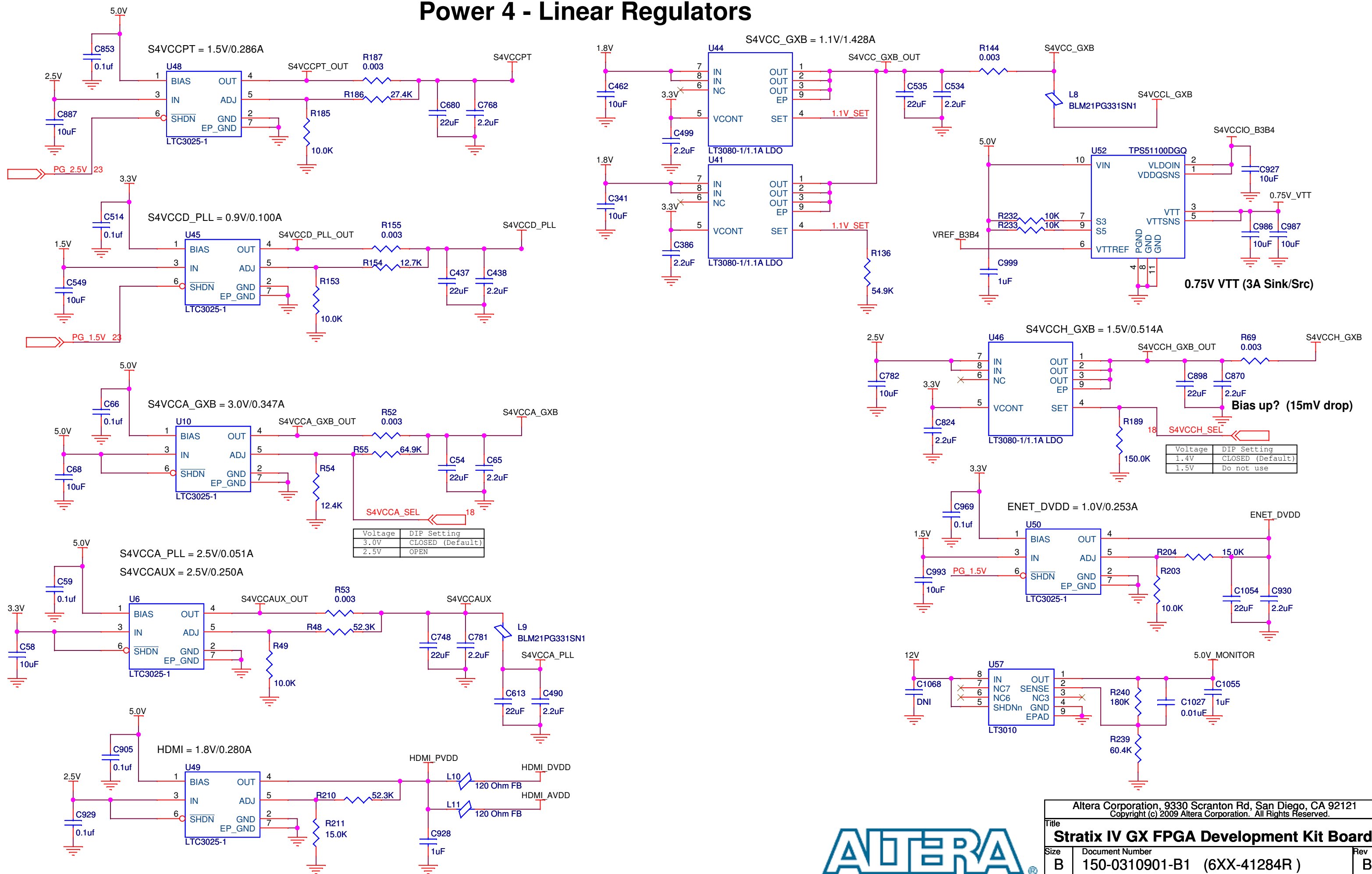


Power 3 - 2.5V, 1.8V, 1.5V

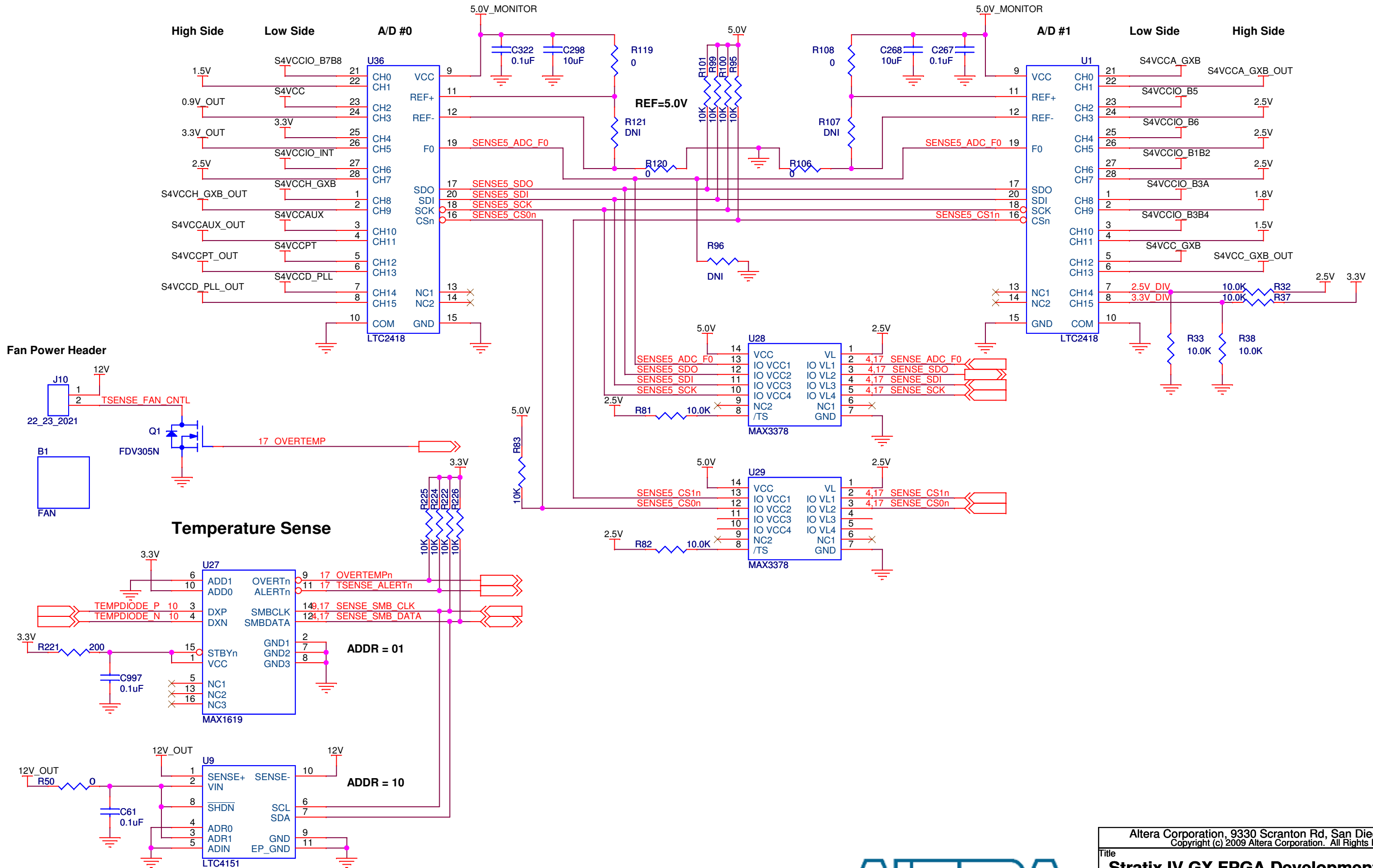
1.8V tracks 1.5V output during ramp-up



Power 4 - Linear Regulators

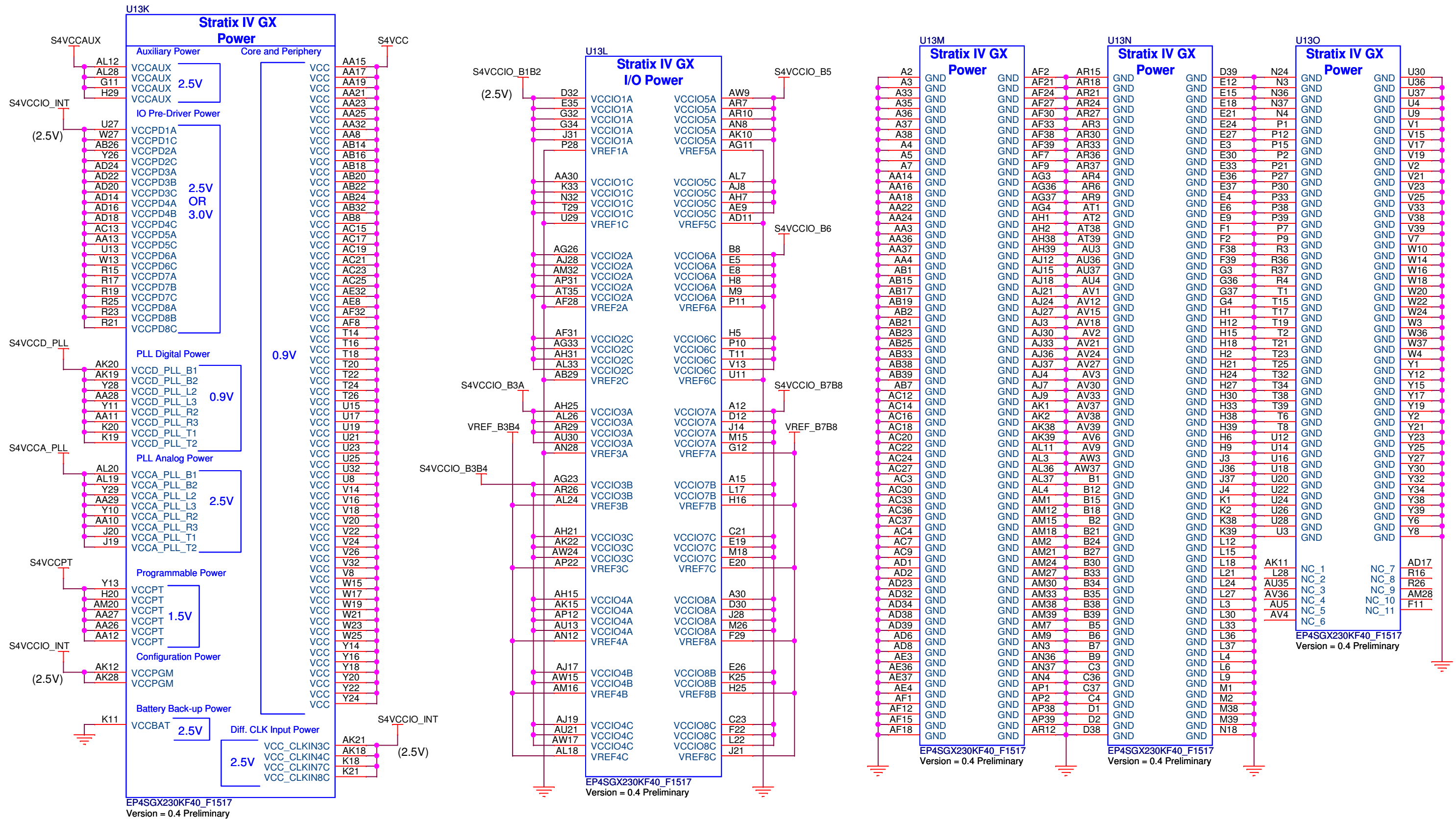


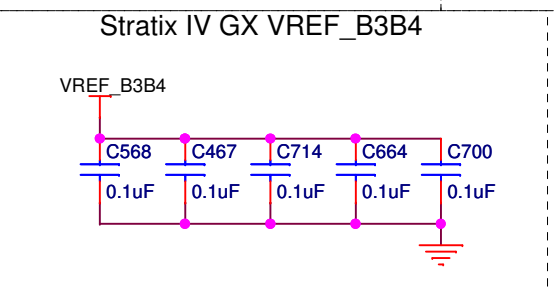
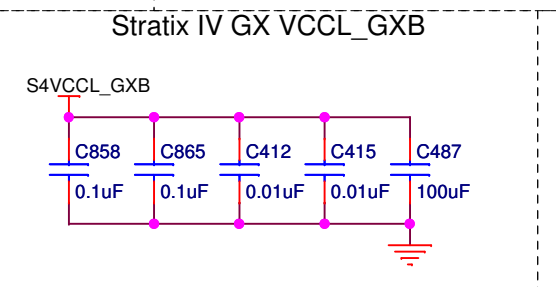
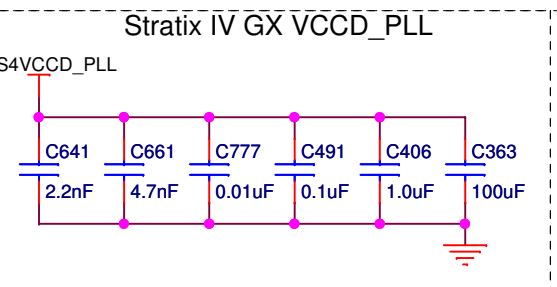
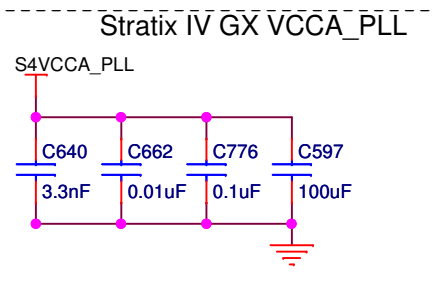
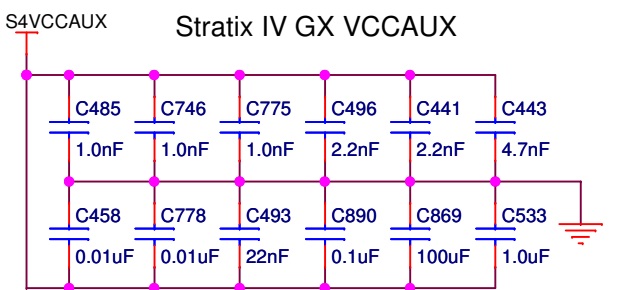
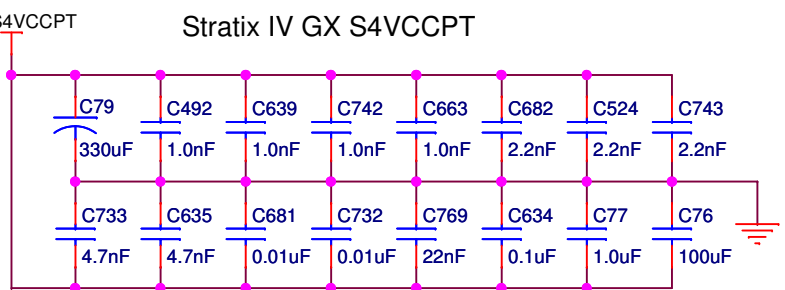
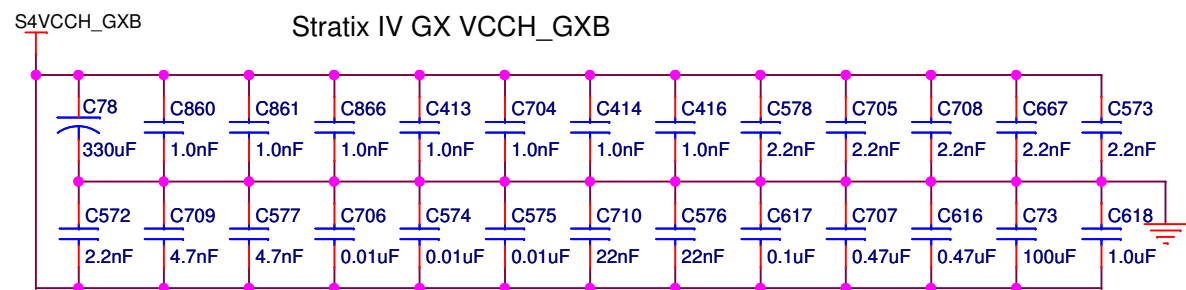
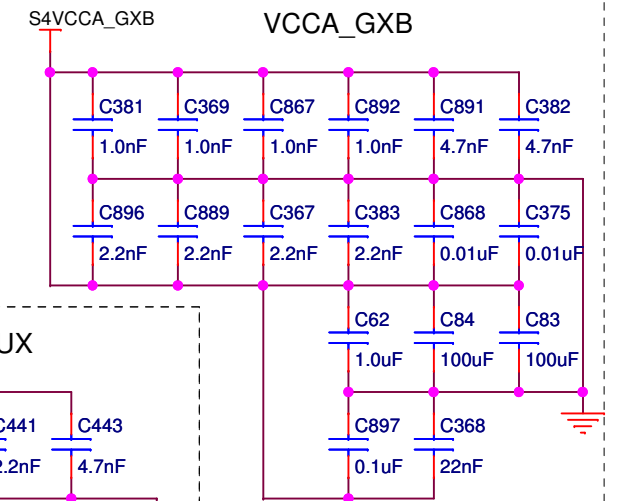
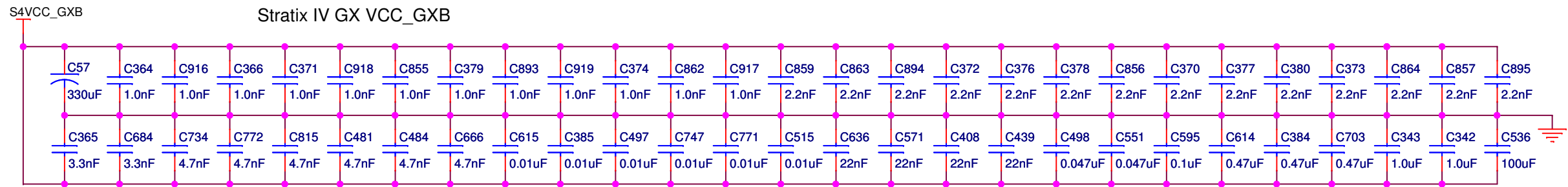
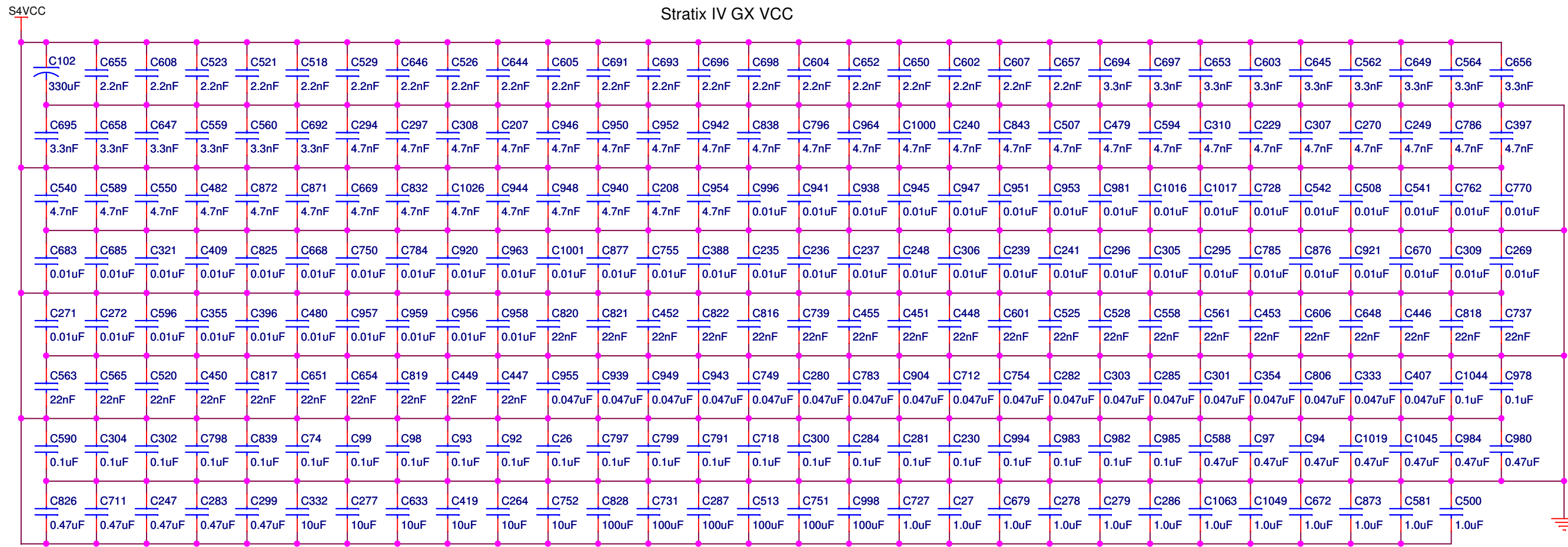
Power & Temp Monitor



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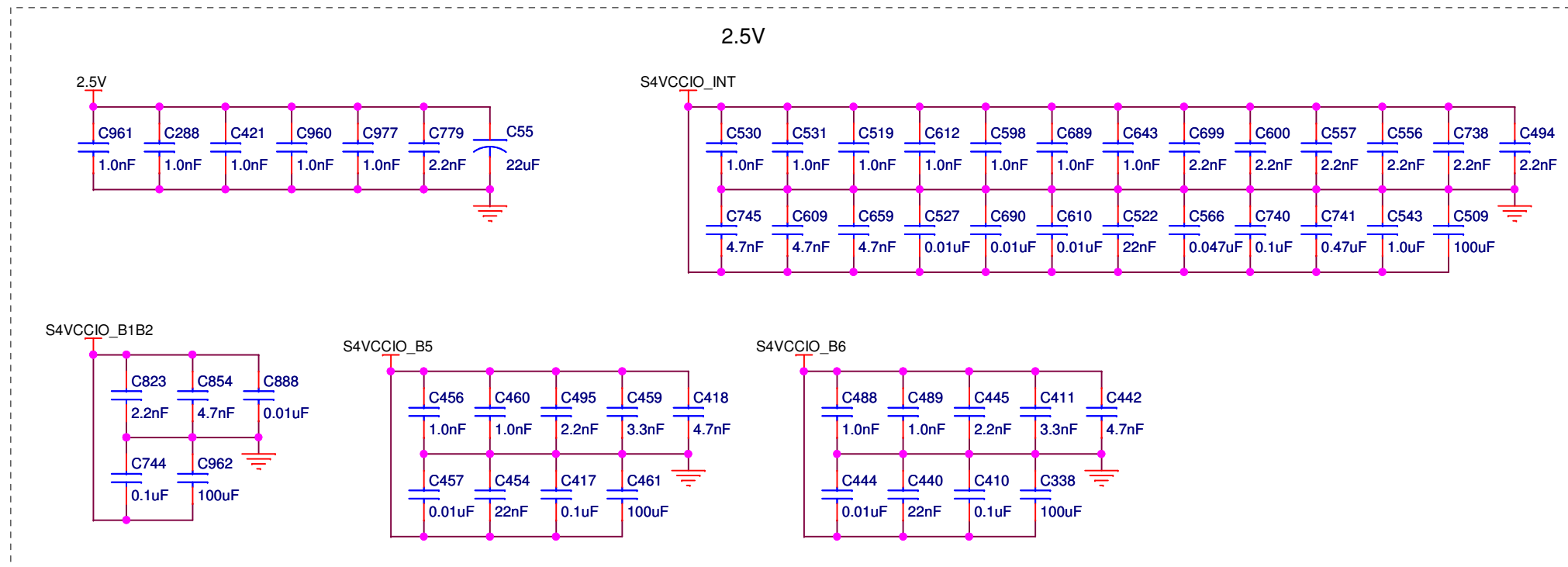
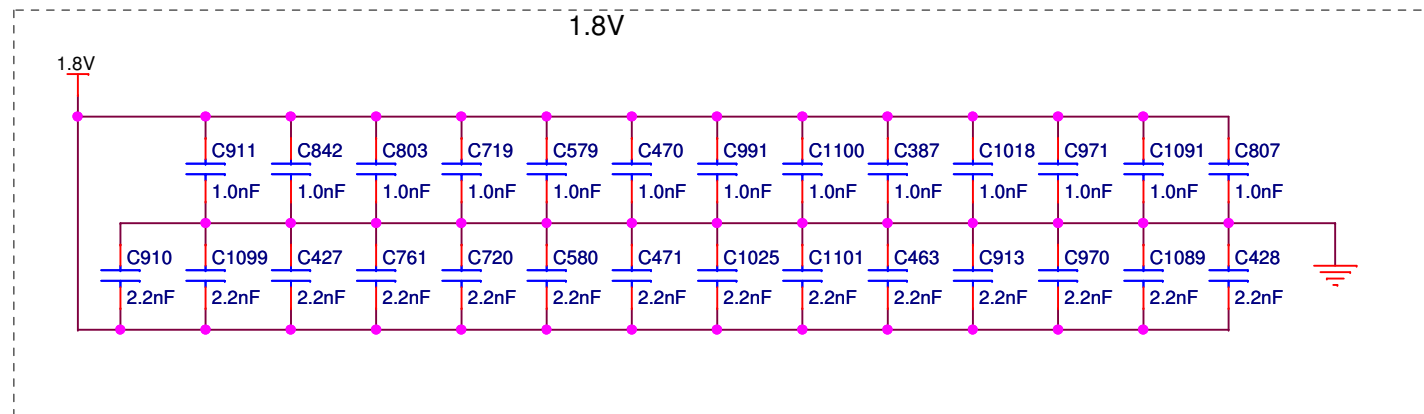
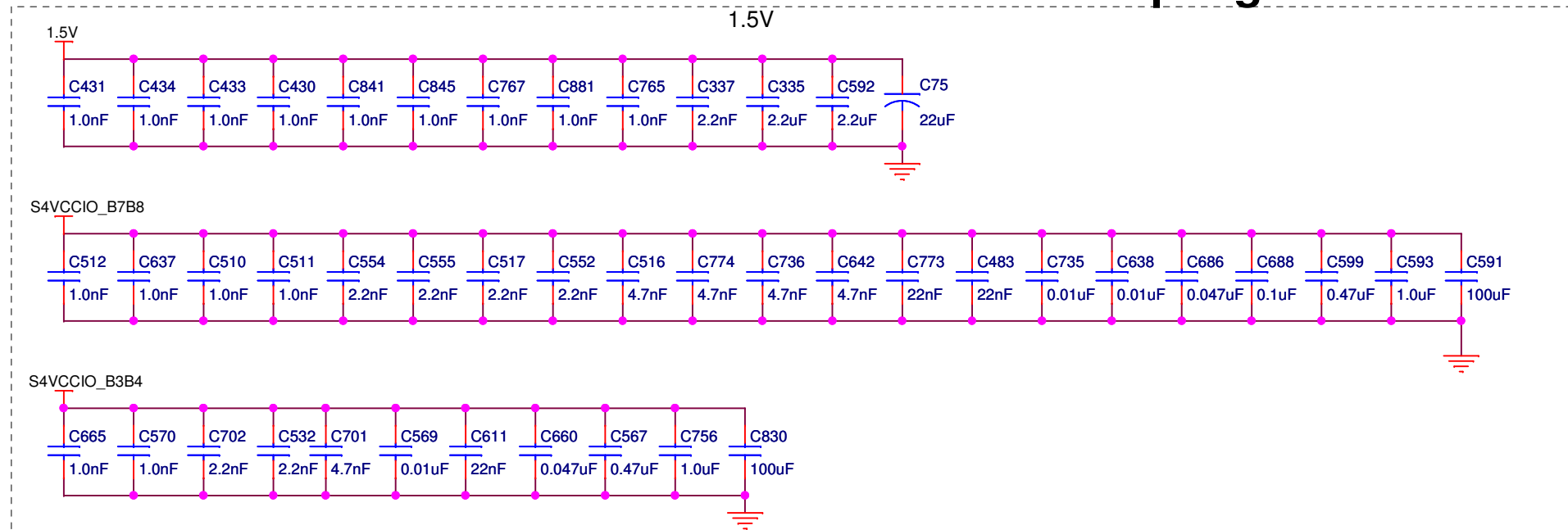
Power 6 - Stratix IV GX Power





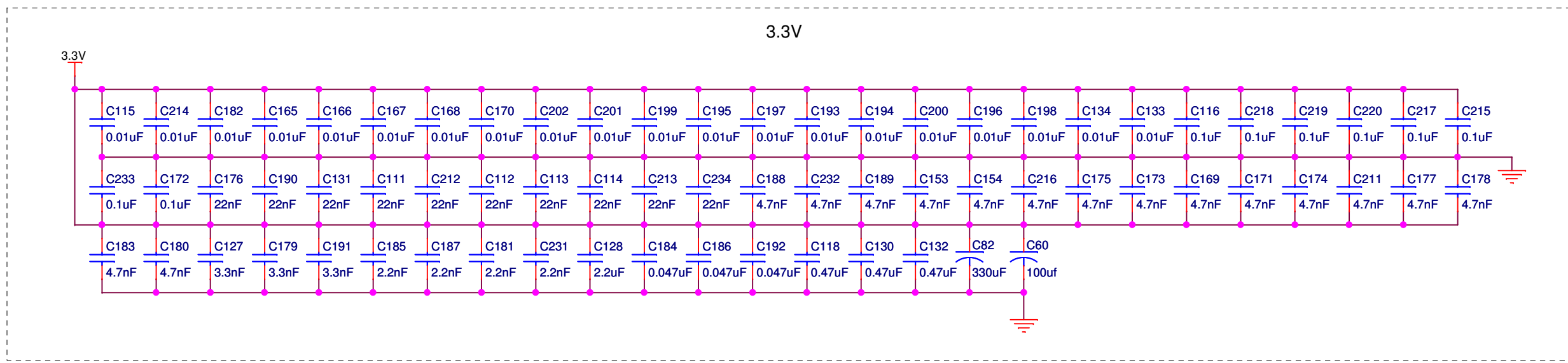
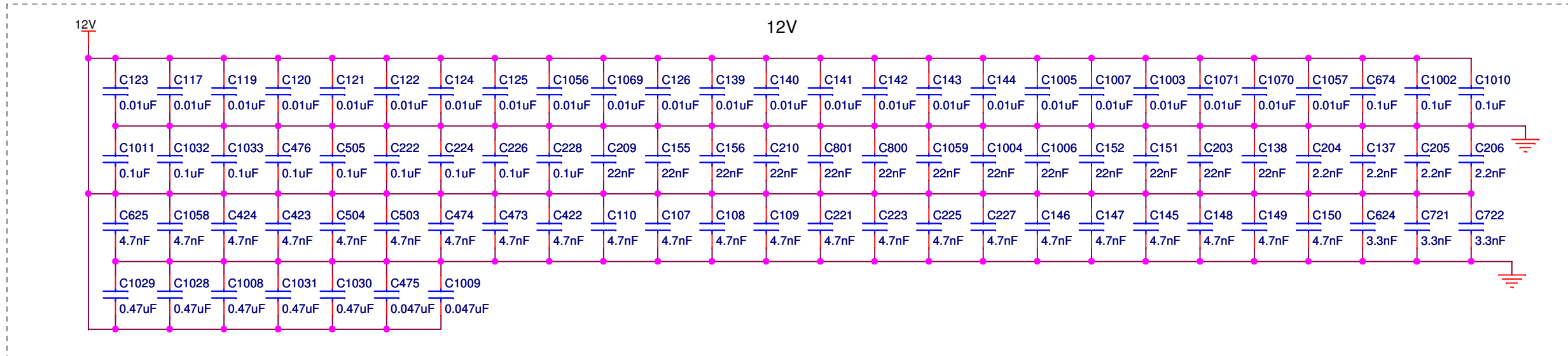
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Decoupling 2



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Decoupling 3



SCREW1	SCREW3	STANDOFF1	SPACER1	PCB1
SCREW2	SCREW4	STANDOFF2	SPACER2	
	SCREW5	STANDOFF3		
		STANDOFF4		



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