Figur 1: The byte (0xBC) is received correctly by the SPI shift_reg
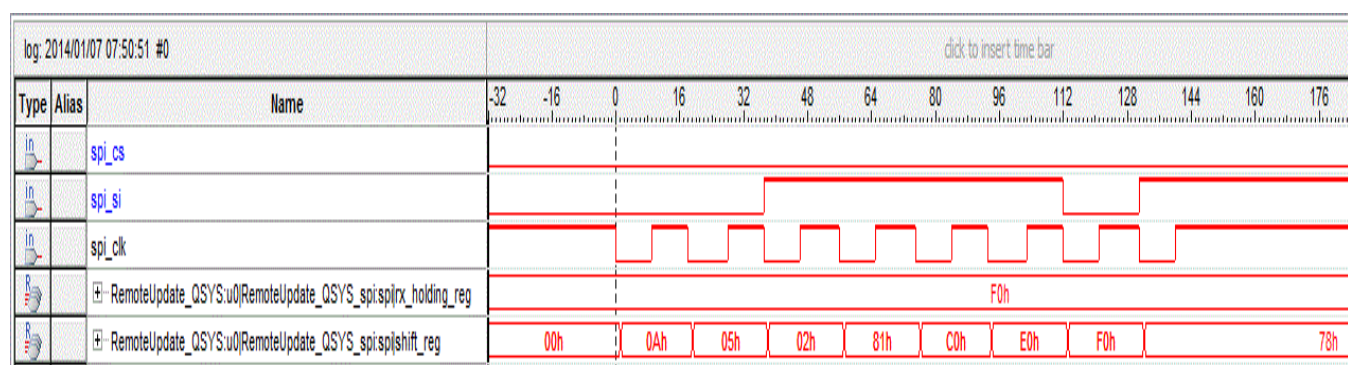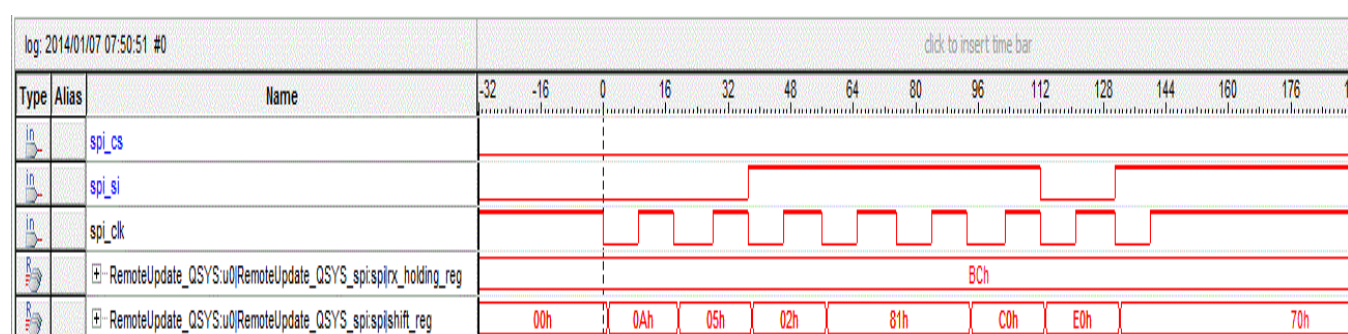

Figur 2: The byte (0xBC) is NOT received correctly by the SPI shift_reg

Figur 3: Again, the byte (0xBC) is NOT received correctly by the SPI shift_reg