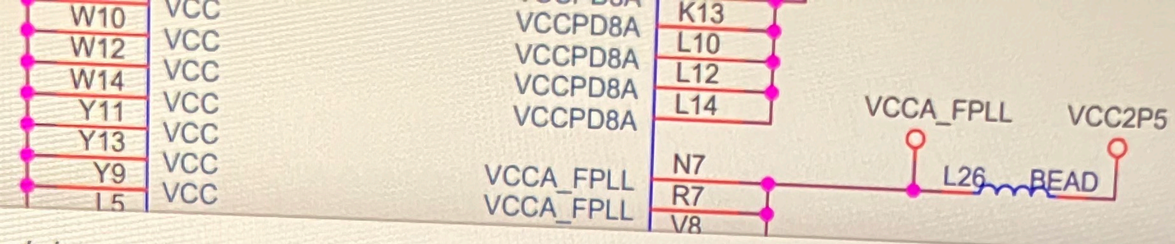
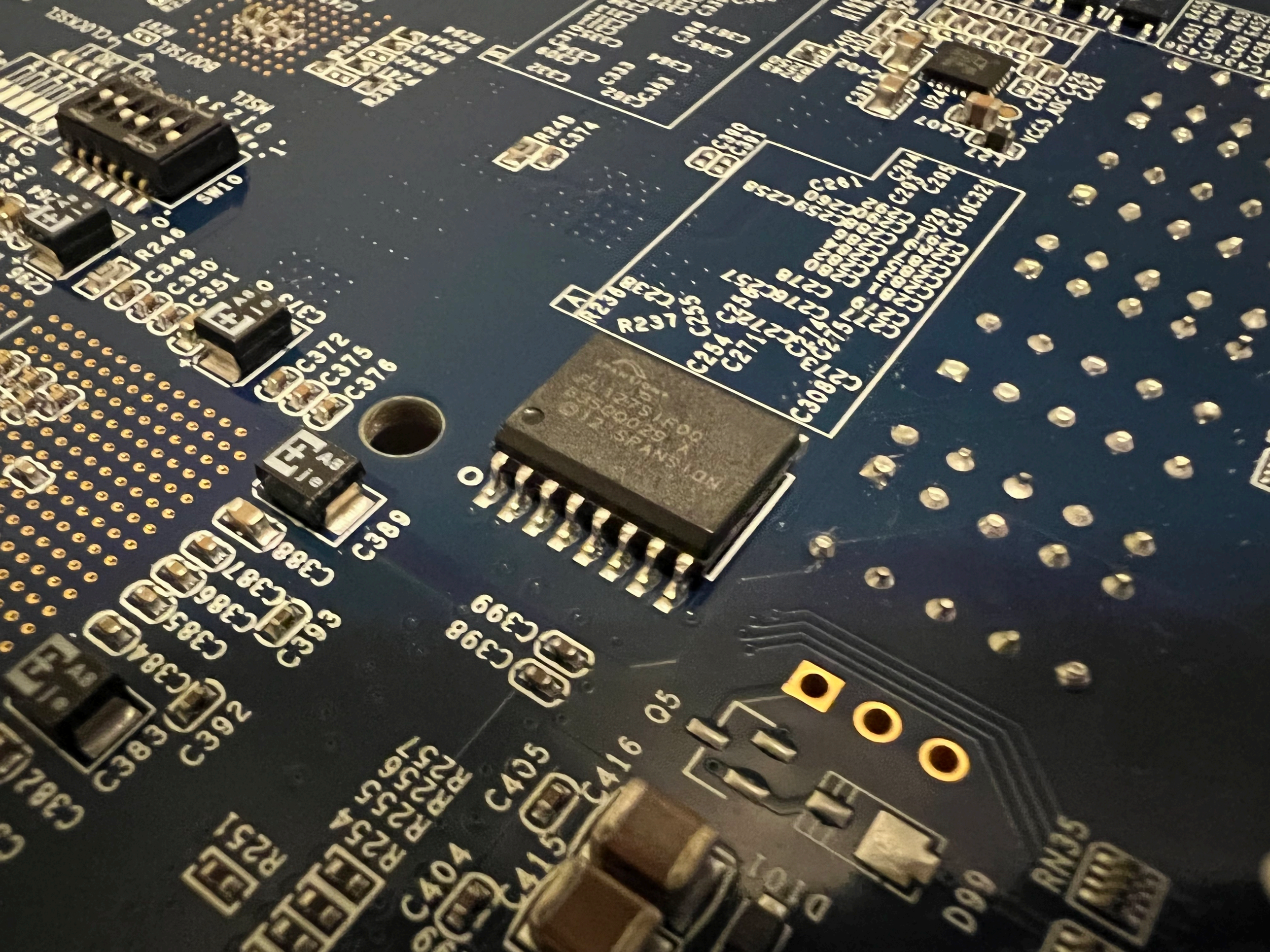


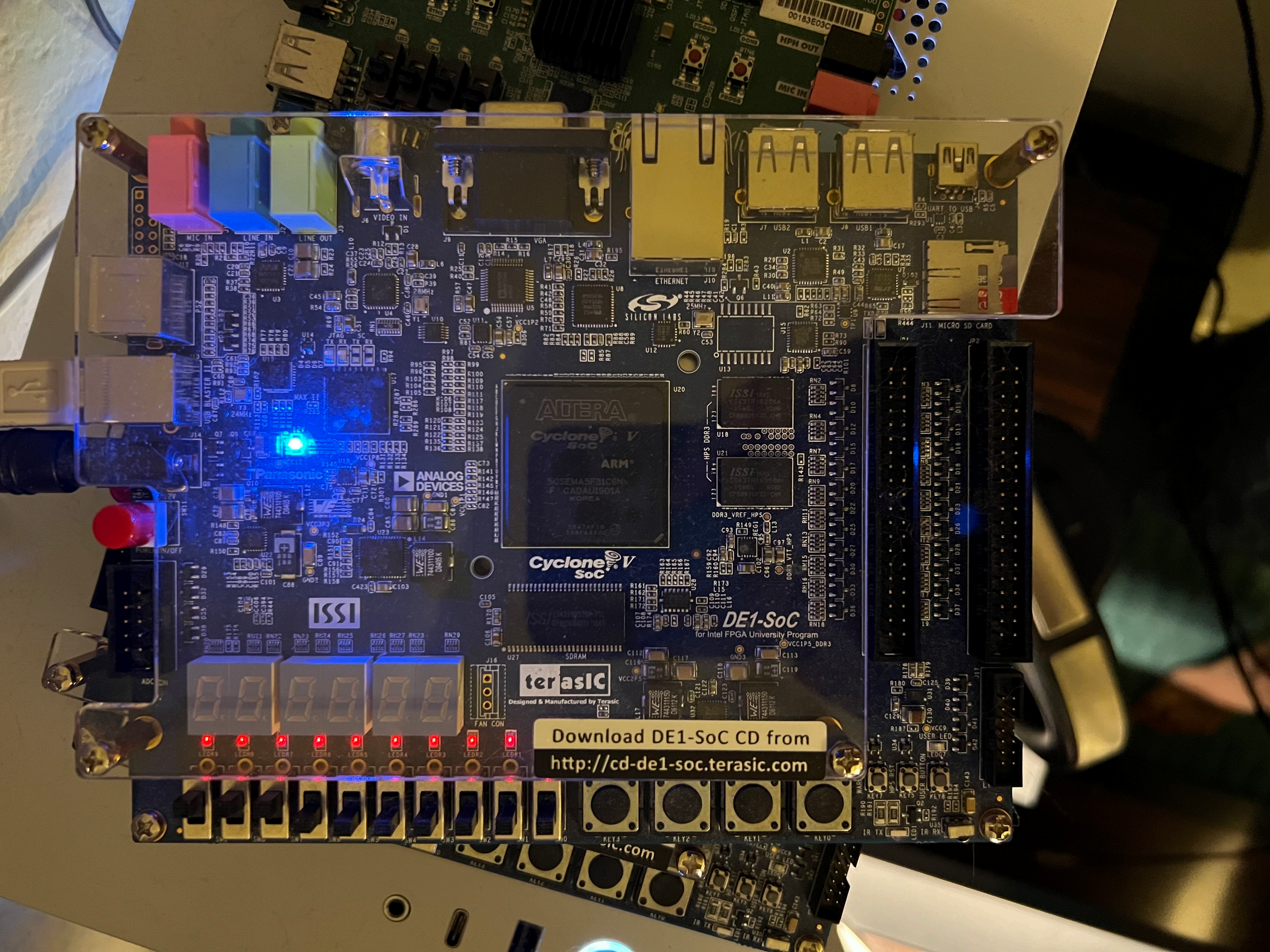
/cygdrive/d/FPGA_Research/Nios2_design/nioscommandlineepcs05_31_22/demo

```
Searching for SOF file:
in .
  SPIProtocol.sof

Info: ***********************************************************************
Info: Running Quartus Prime Programmer
Info: Command: quartus_pgm --no_banner --mode=jtag -o p;SPIProtocol.sof@2
Info (213045): Using programming cable "DE-SoC [USB-1]"
Info (213011): Using programming file SPIProtocol.sof with checksum 0x00D57473 for device 5CSEMA5F31@2
Info (209060): Started Programmer operation at Fri Jun 10 21:59:00 2022
Info (209016): Configuring device index 2
Info (209017): Device 2 contains JTAG ID code 0x02D120DD
Error (209014): CONF_DONE pin failed to go high in device 2. Make sure all communication cables are securely conne
cted, select a different device, check the power on the target system, or make sure all nCE pins are connected to
GND. The Intel FPGA Knowledge Database contains many articles with specific details on how to resolve this error.
Visit the Knowledge Database at https://www.altera.com/support/support-resources/knowledge-base/search.html and se
arch for this specific error message number.
Error (209012): Operation failed
Info (209061): Ended Programmer operation at Fri Jun 10 21:59:03 2022
Error: Quartus Prime Programmer was unsuccessful. 2 errors, 0 warnings
    Error: Peak virtual memory: 4441 megabytes
    Error: Processing ended: Fri Jun 10 21:59:03 2022
    Error: Elapsed time: 00:00:04
    Error: Total CPU time (on all processors): 00:00:01
There are no Nios II processors available which match the values specified.
Please check that your PLD is correctly configured, downloading a new SOF file if necessary.

Haoti@Studystation /cygdrive/d/FPGA_Research/Nios2_design/nioscommandlineepcs05_31_22/demo
$
```

New Volume (E:)

A1445


SW10
R240
C349
C350
C351
C372
C375
C376
C389
C388
C387
C386
C385
C384
C383
C392
C398
C399
C405
C416
Q5
C404
C415
R251
R254
R255
R252
R253
R250
D10
D9
RN35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Cyclone V SoC
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terasIC
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