Failure Analysis Report (Reporte de Análisis de Falla)

Análisis de Falla

Detalles:

Responsable:	Marco Jimenez	**TOP Assy Name:**	CIE-170-5171-405	**FAR # (DDMMAACC):**	31/10/2024
Nombre del componente:	CIE-060-0887-001	**Proyecto:**	CIENA RSP	**Fecha de hallazgo (DDMMYY):**	25/10/2024
Descripción del componente:	IC, PROC, XEON D-1713NTE, 4 CORE, 45W, 3.30 GHZ, 2227-FCBGA, ESD CDM 150V, NON-COMPLIANT TO CPS REQ	**Serial**	B35FD403	**Fecha de cierre (DDMMYY):**	31/10/2024
Estatus:	Replace components	**Estación de falla:**	ICT	**Yield Caido (%):**	

Detalles del defecto:

Unit failed at the ICT shorts stage.
Curve tracer test confirmed that the root cause was a component that is internally shorted.
No manufacturing defects were found in the PCBA.

Para componentes / Ensambles fallados en líneas de producción:

Modo de falla:	SHORTS

Prueba ICT X **Prueba FVT** **Otra:**_____

Mensaje de error en equipo:

```
----------------------------------------
Shorts Report for "shorts".
Tue Oct 22 08:45:43 2024
170-5171-211REV001-40xSFP28(GEN.2)
Board Version: 5171_411
----------------------------------------
Short #1, Thresh 8, Delay 2s Ohms
From: +VDDA_VCCIN_PH2_SW 20466 0
c5048.1
l5117.1
u5257.10
u5257.11
u5257.12
u5257.13
u5257.14
u5257.15
u5257.16
u5257.17
Too many to print.
```

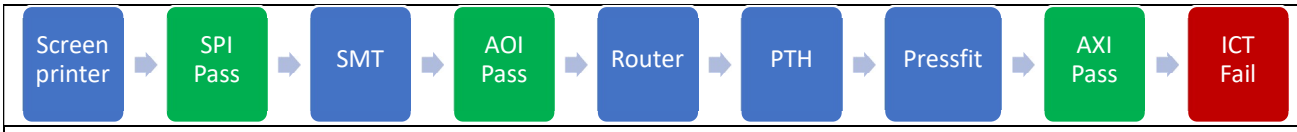


Figure 1: SMT process flow for this board.

State	Enter Time	Exit Time
1509 [CIENA-SMT-UNIT-CREATION PASS]	09/10/2024 07:41:52 ...	09/10/2024 07:41:52 ..
1510 [CIENA-SMT-DEK-BOTTOM PASS]	11/10/2024 11:46:12 ...	11/10/2024 11:46:12 ..
20020 [CESD SMT AOIBottomAutoGUI Ok]	11/10/2024 12:57:38 ...	11/10/2024 12:57:38 ..
20030 [GDL_AOI_AUTO_TEST_BOT PASS]	11/10/2024 12:57:38 ...	11/10/2024 12:57:38 ..
20031 [CIENA-SMT-BOTTOM-BACKFLUSH PASS]	11/10/2024 12:57:39 ...	11/10/2024 12:57:39 ..
1514 [RE-ASSIGN_PO_PN_BOTTOM_TO_SMTT PASS]	11/10/2024 01:16:42 ...	11/10/2024 01:16:42 ..
1513 [CIENA-SMT-DEK-TOP PASS]	11/10/2024 01:17:06 ...	11/10/2024 01:17:06 ..
20060 [CESD SMT AOITopAuto GUI]	11/10/2024 05:01:25 ...	11/10/2024 05:01:25 ..
20070 [GDL_AOI_AUTO_TEST_TOP PASS]	11/10/2024 05:01:25 ...	11/10/2024 05:01:25 ..
20071 [20071 - CESD-SMT-Top Backflush]	11/10/2024 05:01:26 ...	11/10/2024 05:01:26 ..
5022 [RE-ASSIGN_PO_PN_TOP_TO_400 PASS]	12/10/2024 01:45:24 ...	12/10/2024 01:45:24 ..
838 [CIENA-SMT-ROUTER PASS]	12/10/2024 01:46:13 ...	12/10/2024 01:46:13 ..
1517 [CIENA-SMT-WAVE-INSPECTION PASS]	12/10/2024 01:48:47 ...	12/10/2024 01:48:47 ..
1512 [CESD-SMT-PTH PASS]	12/10/2024 01:49:50 ...	12/10/2024 01:49:50 ..
1606 [CESD SMT-PRESSFIT- NPI]	12/10/2024 01:55:44 ...	12/10/2024 01:55:44 ..
20170 [CESD SMT 5DXAuto GUI]	12/10/2024 07:04:33 ...	12/10/2024 07:04:33 ..
20180 [GDL_AXI_AUTO_TEST PASS]	12/10/2024 07:04:33 ...	12/10/2024 07:04:33 ..
20215 [GDL_ICT_AUTO_TEST FAIL]	22/10/2024 01:15:14 ...	22/10/2024 01:15:14 ..
7330 [CIENA-SMT-EXP-DEBUG-IN]	22/10/2024 08:21:59 ...	22/10/2024 08:21:59 ..

Figure 2: Flexflow board history.

Introduction

The unit failed at ICT due to low impedance in the signal +VDDA_VCCIN_PH2_SW.

Debug methods allowed us to narrow down the defect to an ASIC.

There were no visual manufacturing defects in the board, so component analysis is needed.

Analysis

To find the defect, the following information was gathered.

Unit history

As per the Flexflow record, the unit went through its normal SMT route, and failed at the ICT , this is shown in Figure 1 as a diagram and Figure 2 shows the board history from Flexflow.

As such, we can state the following:

- The unit had not been yet powered on when the issue arose.
- The unit had no visual manufacturing defects (AOI and AXI passed).

Test

As per the unit history, the unit was tested in ICT; the following issue arose:

Signal	Defect
+VDDA_VCCIN_PH2_SW	Low impedance

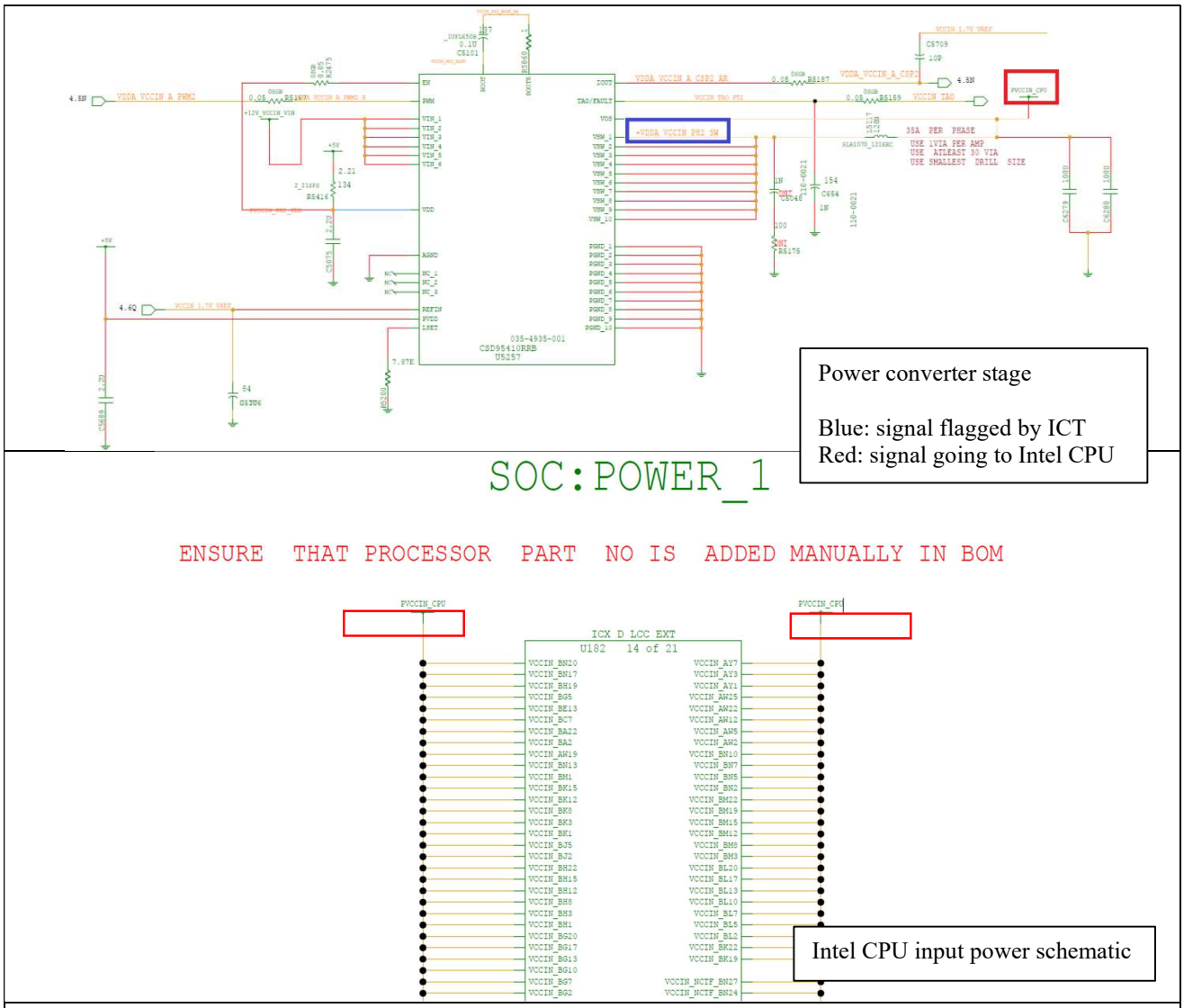


Figure 3: Circuit schematic of signals under analysis.

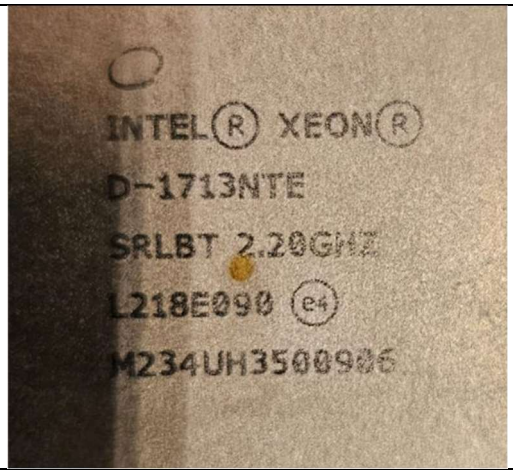


Figure 4: Component top marking.

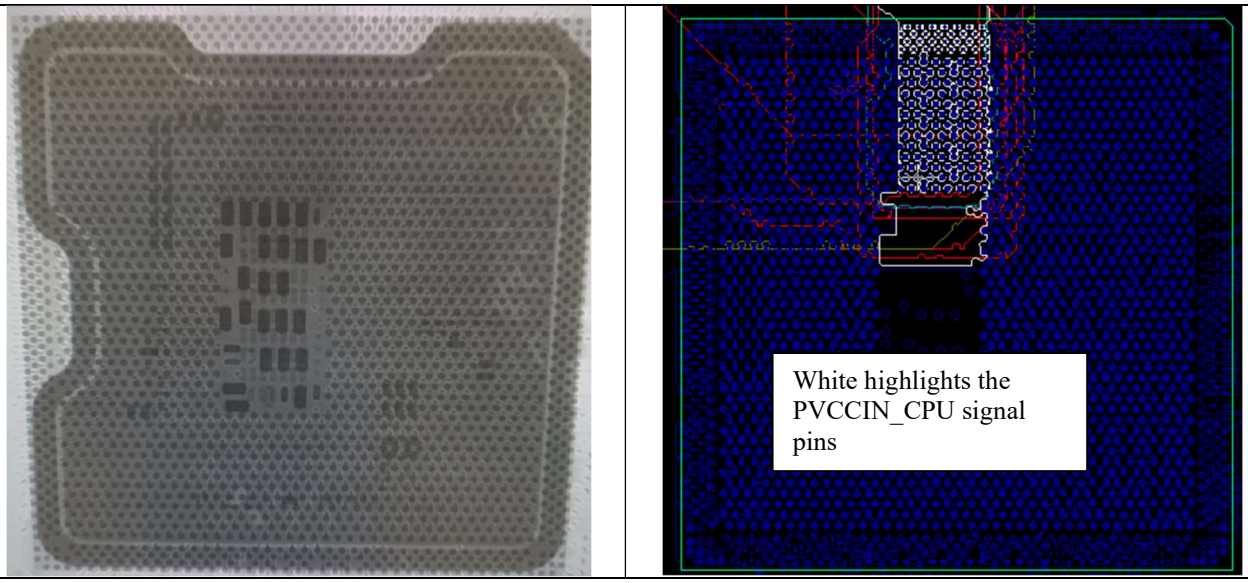


Figure 5: XRAY image of the component under analysis installed in the PCBA, no solder shorts are in presenc– side to side comparison with Gerber file where pins under analysis are highlighted.

PCBA Debug steps

In Figure 3, the circuit of the affected signal is shown, the affected signal is highlighted in a red rectangle, the signal flagged by ICT is highlighted with the blue rectangle. In the next schematic snippet, the input stage of the PVCCIN_CPU to the U182 BGA is shown.

The following debug sequence was done:

1. We performed double validation with visual inspection, discarding the possibility of an inverted component or incorrect top marking, no visible defects were found confirming the results from AOI, as shown in Figure 4.

2. We performed double validation with manual XRAY, discarding solder shorts confirming the results from AXI, as shown in Figure 5

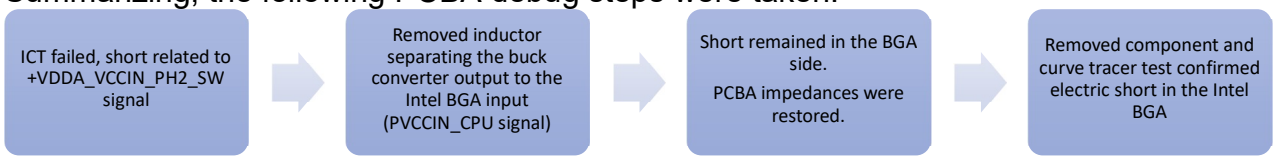
3. In order to isolate the short between power supply and load, the inductor L5117 was removed from the PCBA.

4. After removing L5117, the impedance of the +VDDA_VCCIN_PH2_SW (blue rectangle) signal was restored, effectively isolating the issue at U182.

5. Board was sent to remove U182.

6. After U182 removal, the PVCCIN_CPU (red rectangle) node was measured in the bare pads of the PCBA, and the impedance was restored, further confirming that the low impedance was located at the IC at U182.

Summarizing, the following PCBA debug steps were taken:



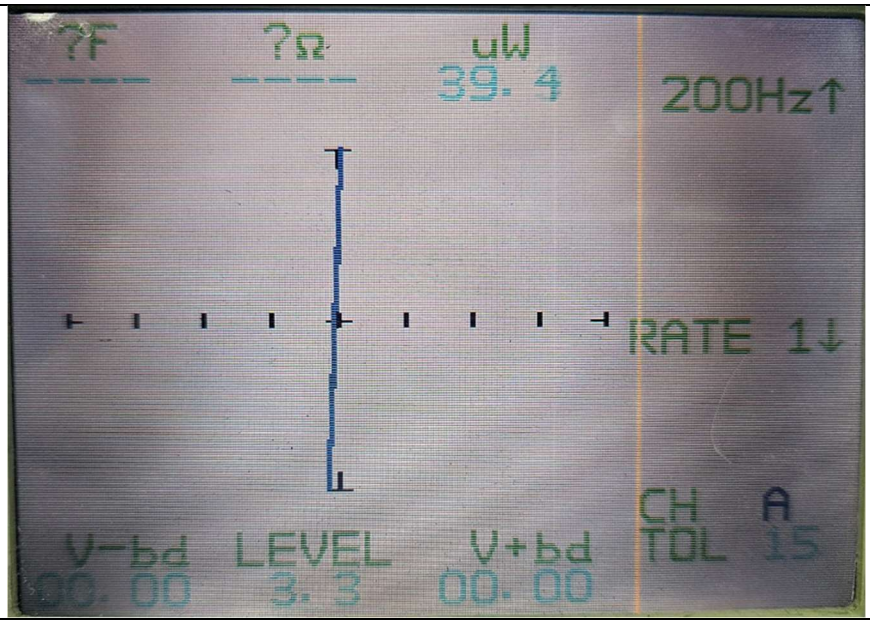


Figure 6: Curve trace test results for pin BL27 vs GND.

Component level analysis

In order to verify if the component was internally damaged, curve tracer test was performed in the component, specifically in pin BL27 vs GND. The result is in Figure 6.

It is evident that the Intel BGA (U182) has an internal short to GND in pin the pins corresponding to PVCCIN_CPU signal.

After the previous debug sequence & the component level analysis, we reach the following conclusions.

Conclusions

- No noticeable manufacturing defects could be found in the board.
- The defect is located at the ASIC, curve tracer test confirmed the short.
- To determine the exact nature of the defect, further component analysis of this IC is required.