Memory Replacement Guideline and Advanced Memory Test for DSG Commercial Platform Server BIOS

Technical Paper

Revision 2.1

May 2023

Document Revision History

Date	Revision	Changes
March 2021	0.5	Initial release of the document.
April 2021	1.0	Wording clarification.
April 2021	1.1	• Added OEM BIOS POST Event and Memory Error Extension to SEL Log entry table. • Removed ED1 table. • Added POST Package Repair Runtime Request to SEL examples.
July 2021	1.2	Corrected hexadecimal example for bits 7 and 9.
September 2021	1.3	Added hexadecimal in contrast to decimal for the Intel® Server Configuration Utility versions.
September 2021	1.4	Added hexadecimal in contrast to decimal for Intel Integrator Toolkit (ITK) versions.
October 2021	1.5	• Clarify AMT error vs AMT completion with error. • Add PPR and DIMM replacement headings.
December 2021	1.6	Clarify leading 'A' in first nibble in ED1.
January 2022	1.7	• Correct version of ITK that uses hex instead of decimal. • Marking 04h Advanced Memory Test Completion without Error as non-functional.
March 2022	1.8	• Added description of what an ECC and UCE are. • Added details of enhancement on DSG BIOS versions. • Added further details or memory replacement guidelines.
May 2022	1.9	• Updated Section 1. • Added more details in Section 2. • Added images to Section 5.1. • Added images and more details to Sections 5.2.1, 5.2.2 and 5.2.3. • Added images and more details to Section 7.2. • Merged AMT Fail and PPR Finish; added more details in Sections 7.3.1.1, 7.3.1.2, 7.3.1.3. • Updated Appendix B. • Language and format edits throughout the document.
June 2022	2.0	• Added Section 2.3. • Minor language and style edits.
May 2023	2.1	• Added guidelines and recommendations for CE.

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1. Introduction

This document provides information to understand memory failures and identify memory errors. It also serves as a guide to identify when to replace a memory Dual In-line Memory Module (DIMM) on Intel® Server Systems.

An error correction code (ECC) refers to errors that are self-correcting. Depending on the reliability availability serviceability (RAS) configuration of the memory, the integrated memory controller (IMC) may take the affected DIMM offline. ECC correctable errors (CE) represent a threshold overflow for a given DIMM, within a given time frame.

An uncorrectable error (UCE) refers to uncorrectable errors related to a failing DIMM that must be repaired or replaced.

2. What to Do When a DIMM Error Occurs

Users can check for memory errors in the system event log (SEL) following any of these methods:

1. Run the Intelligent Platform Management Interface (IPMI) command `ipmitool sel list`.
2. Go to the Integrated Baseboard Management Controller (BMC) Web Console using a valid IP address and navigate to **Server Health > Event Log**.
3. Run the Intel® Server Configuration Utility command `syscfg /sbmcdl /savebmcdebuglog Public <filename>.zip`.
4. Run the Intel® Server Information Retrieval Utility command `sysinfo`; and in the folder `LogFiles`, open the file `sysinfo_log.txt`.
5. Collect the SEL using Redfish* `URI /redfish/v1/Systems/{ID}/LogServices/SEL`.

2.1 Examples of Memory Errors Logged in the SEL

2.1.1 Memory Correctable Error (CE)

```
0002 - RID:0002 RT:02 TS:59D2B15F GID:0033 ER:04 ST:0C S#:02 ET:6F ED:A0 01
   10 EX:00 FF FF FF FF FF FF FF
0002 - RID:0002 TS:10/02/2017 21:36:31 SN:Mmry ECC Sensor ST:Memory
   ED:Correctable ECC error ET:Asserted EC:OK
```

2.1.2 Memory Uncorrectable Error (UCE)

```
0018 - RID:0013 RT:02 TS:5E4FBDA8 GID:0033 ER:04 ST:0C S#:02 ET:6F ED:A1 00
   22 EX: 01 FF FF FF FF FF FF FF
0018 - RID:0013 TS:02/21/2020 11:23:20 SN:Mmry ECC Sensor ST:Memory
   ED:Uncorrectable ECC error ET:Asserted EC:Non-Critical
```

2.2 Recommended Action When a Correctable Error Is Logged

A. If performance is not impacted, no further action is required. The error was corrected by the ECC mechanism.
Recommended action–Increase the threshold at which the SEL records correctable errors. The BIOS defaults to <10>; recommendation is <500> when there is no performance impact
`F2 > Advanced > Memory Configuration > Memory RAS and Performance Configuration > Correctable Error Threshold <500>`

B. If system performance has degraded, test the memory for potential issues
Recommended action–Run the Advanced Memory Test. See Chapter 5 for details

2.3 Recommended Action When an Uncorrectable Error Is Logged

A. If AMT has been enabled previously, reboot the system. AMT will test and attempt to repair the DIMM automatically.
B. If AMT has not yet been enabled, see Chapter 5 for instructions on enabling and running AMT.
C. If AMT is able to use POST Package Repair (PPR) to repair the DIMM, no further action is required.
D. If AMT or PPR fail to repair the DIMM, further actions may be required. Details are in Chapter 5.

3. Tune the Threshold for Correctable Error ECCs

Correctable Errors are well tolerated. The Correctable Error Threshold is modifiable, allowing a number of CEs to be disregarded before logging an event.

The threshold defaults to 10, which historically was useful for older systems on DDR3 memory, with less than 8 GB of total memory. Current systems running DDR4, and greater than 8 GB of total memory, should be adjusted for the current workload.

By default, the threshold accumulates errors on a per-rank basis. This means that errors occurring in entirely separate banks or integrated circuits (ICs) will be grouped, as though they were related.

You may also increase the accuracy of the location of CEs, by enabling a per-bank threshold:

```
F2 > Advanced > Memory Configuration > Memory RAS and Performance Configuration >
Trigger SW Error Threshold <Enabled>
```

The actual number of banks per IC, and IC per rank, varies by memory vendor. The recommended bank-per rank of

```
F2 > Advanced > Memory Configuration > Memory RAS and Performance Configuration >
Sparing SW Error Threshold <4>
```

can be adjusted based on specifications from your memory vendor

The CE count is maintained in hardware registers with a “leaky bucket” algorithm. As time passes with no new CE, the total accumulated count is reduced. The exact time interval is non-linear and varies with the DRAM running clock. Assuming a clock of 2400 MT/s, the total collected error count decreases around 1 per 24 hours. This can be adjusted under:

```
F2 > Advanced > Memory Configuration > Memory RAS and Performance Configuration >
Correctable Error Time Window
```

4. Advanced Memory Test

4.1 Advanced Memory Test (AMT)

Intel introduced Advanced Memory Test (AMT) features in the Datacenter Solutions Group (DSG) BIOS and firmware stack. AMT was included in BIOS revision 02.01.0014 for the Intel® Server Systems S2600BP, S2600WF, and S2600ST; and in BIOS revision 22.01.0097 for the Intel® Server System S9200WK. AMT was included at launch in the Intel® Server Systems D50DNP, D50TNP, M50FCP, and M50CYP.

See Chapter 5 for steps to enable AMT, and how to monitor AMT in the System Event Log (SEL).

For an overall description of AMT, including input parameters, see the reference document listed in Table 4-1.

Table 4-1. Reference Documentation

Document	Document Number or Location
Advanced MemTest Application in the Server BIOS Memory Reference Code	https://cdrdv2.intel.com/v1/dl/getContent/566767

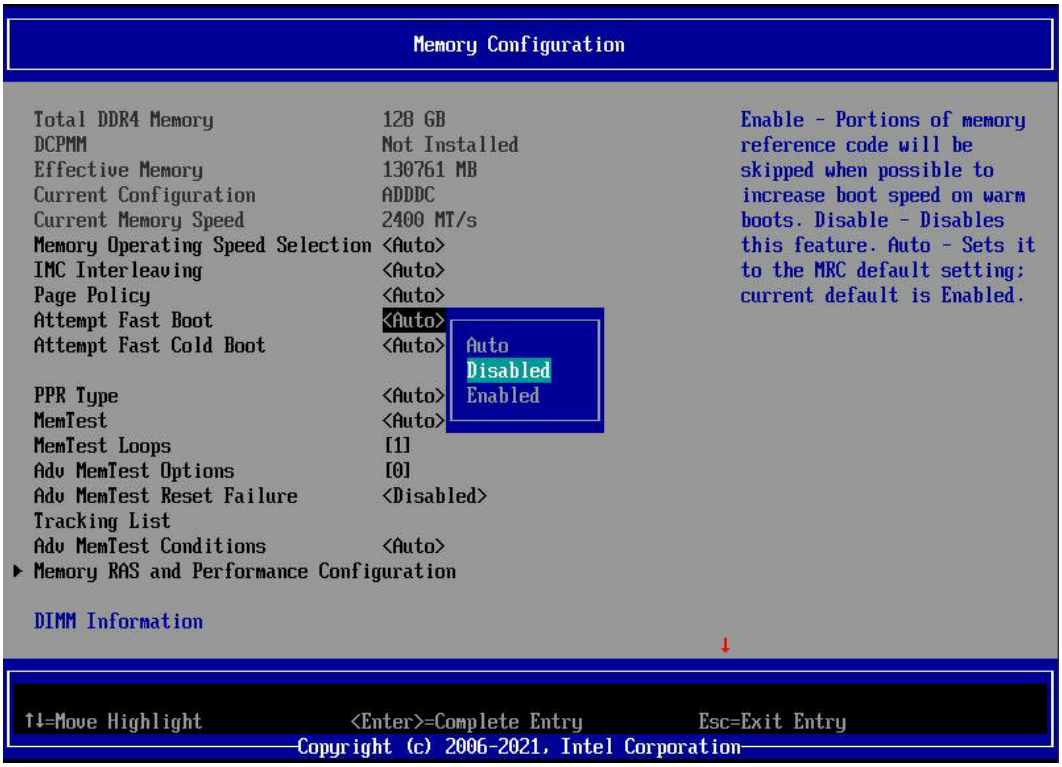
5. AMT Enablement Through the BIOS Setup Utility

5.1 Required Settings

The AMT feature is enabled through the BIOS setup utility for Intel server systems, by choosing the required settings listed in Section 5.1.1. The settings are found in the BIOS setup utility menu, which is accessed by pressing F2 during boot.

5.1.1 Memory Configuration and Server Management

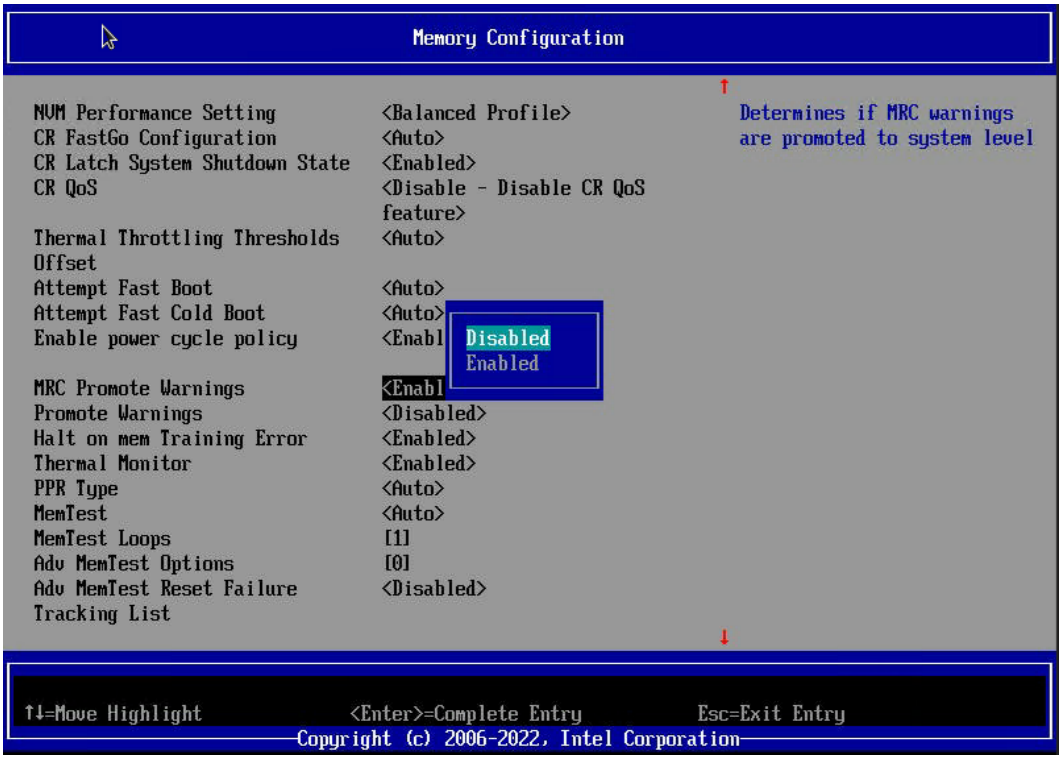
Advanced > Memory Configuration > **Attempt Fast Boot [Disabled]**



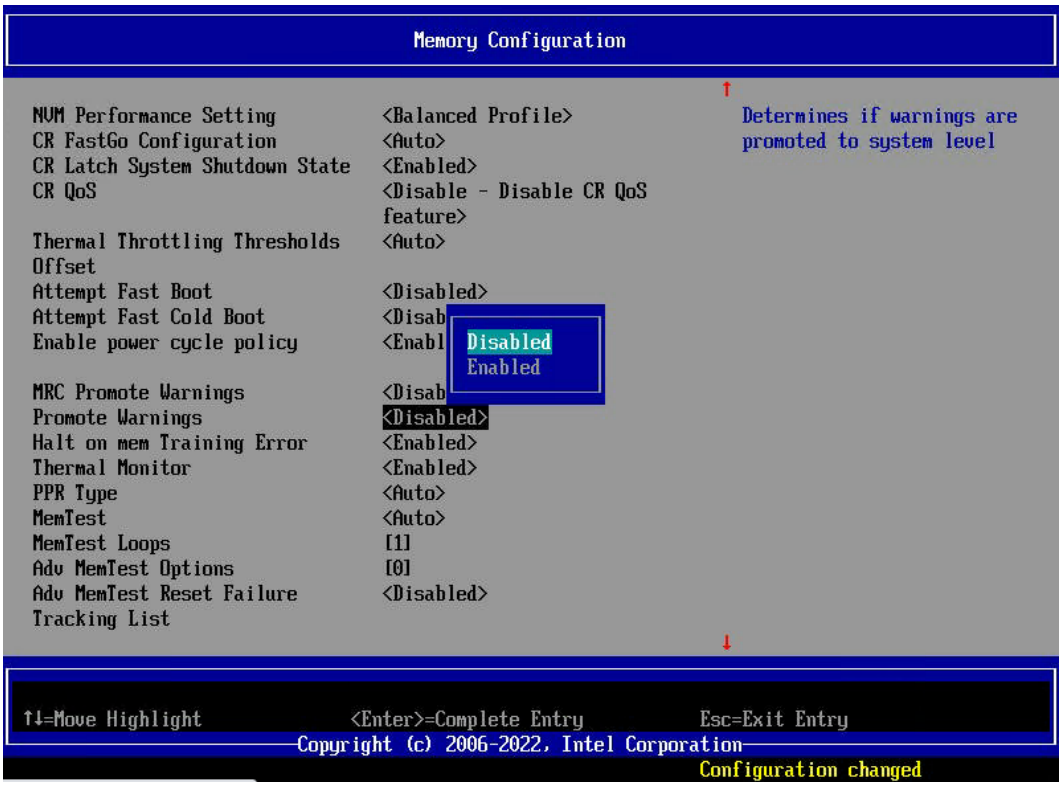
The fast boot feature must be disabled to run an AMT. If fast boot is enabled, this configuration bypasses the AMT initialization.

Advanced > Memory Configuration > **Attempt Fast Cold Boot [Disabled]**

Advanced > Memory Configuration > **MRC Promote Warnings [Disabled]**

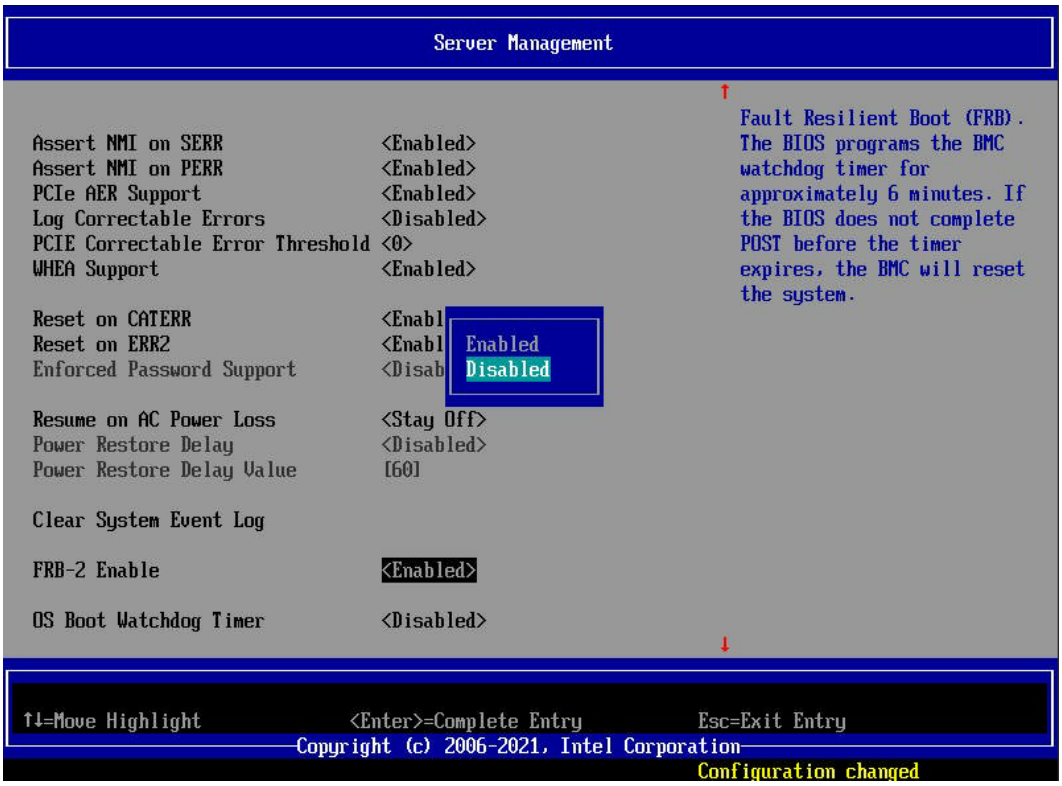


Advanced > Memory Configuration > **Promote Warnings [Disabled]**



Advanced > Memory Configuration > **MemTest [Enabled]**

Server Management > **FRB-2 Enable [Disabled]**



An AMT may run longer than six minutes, which may trigger a watchdog timeout. Disabling FRB-2 allows the test to complete without triggering the watchdog timeout.

5.2 Optional Settings

In addition to the required settings, three optional settings are available to control the functioning of AMT and POST Package Repair (PPR) features.

5.2.1 MemTest Loops

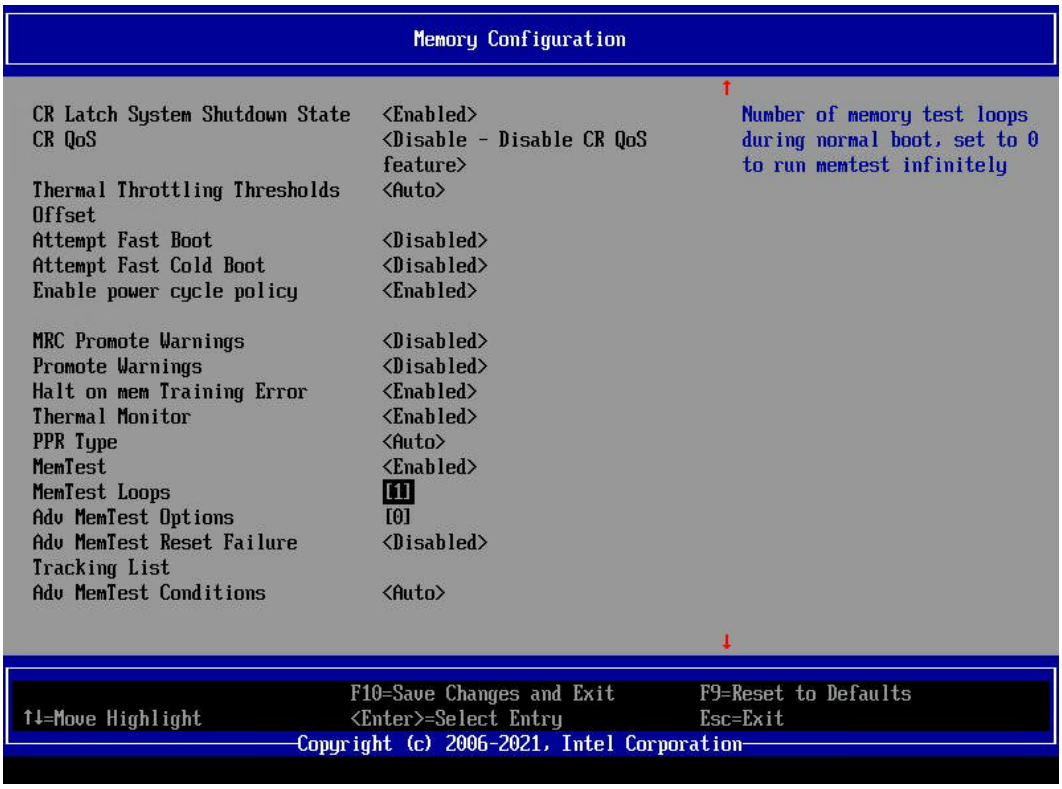
MemTest Loops sets the number of times to loop through the memory test.

Default is [1].

Setting to [0] causes the memory test to run continually.

Go to Advanced > Memory Configuration > **MemTest Loops [ ]**

- Set loops to **1**, for all field and production applications.



5.2.2 PPR Type

PPR Type determines the type of action for PPR to take.

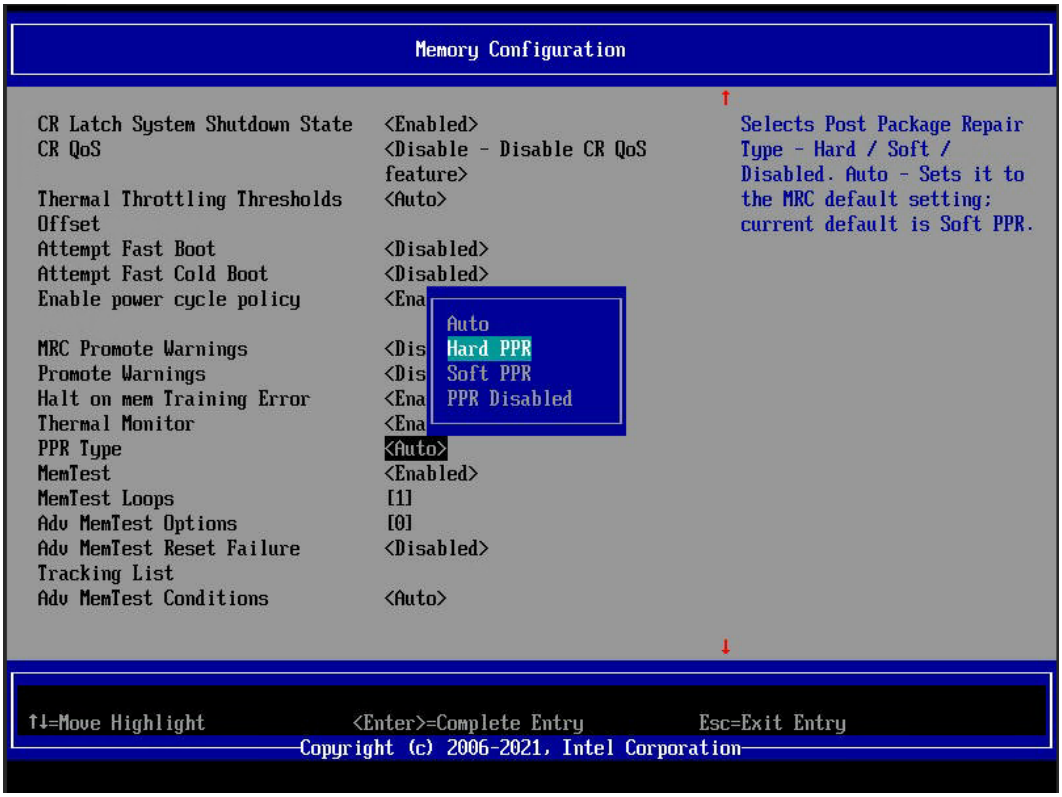
Default is [Soft].

PPR Type [Hard] removes the failing cell permanently to prevent future use.

PPR Type [Soft] only marks the failing cell as temporarily inactive.

Go to Advanced > Memory Configuration > **PPR Type [ ]**

- Use **[Hard]** for production use. The [Soft] option is meant for parameter testing purposes only. See Chapter 6 for more information.



5.2.3 Advanced MemTest Options

Advanced MemTest Options are used to perform direct memory tests by vendor and bit length. This option is automatic by default and does not require the user to select any, unless the user wants to perform a specific test.

Advanced MemTest Options are bit-mask-based, and in hexadecimal format.

Bit 0: XMATS8
Bit 1: XMATS16
Bit 2: XMATS32
Bit 3: XMATS64
Bit 4: WCMATS8
Bit 5: WCMCH8
Bit 6: GNDB64
Bit 7: MARCHCM64
Bit 8: LTEST_SCRAM // Reserved for internal use
Bit 9: LINIT_SCRAM // Reserved for internal use
Bit 10: RANGE_TEST_SCRAM // Reserved for internal use
Bit 11: TWR
Bit 12: DATA_RET
Bit 13: MATS8_TC1
Bit 14: MATS8_TC2
Bit 15: MATS8_TC3
Bit 16: SKHYNIX
Bit 17: SAMSUNG
Bit 18: MICRON
Bit 19: SCRAM_X2

For example, to enable the Samsung* test (bit 17), input **[20000]** in the Options field.

Note: Earlier versions of the Intel Server Configuration Utility and Intel® Integrator Toolkit use decimal instead of hexadecimal.

Intel Server Configuration Utility versions 14.x and earlier read and write as decimal. Example:

```
# /usr/bin/syscfg/syscfg /bcs "" "Adv MemTest Options" 131072
```

Intel Server Configuration Utility versions 15.x and later read and write as hexadecimal. Example:

```
# /usr/bin/syscfg/syscfg /bcs "" "Adv MemTest Options" 0x20000
```

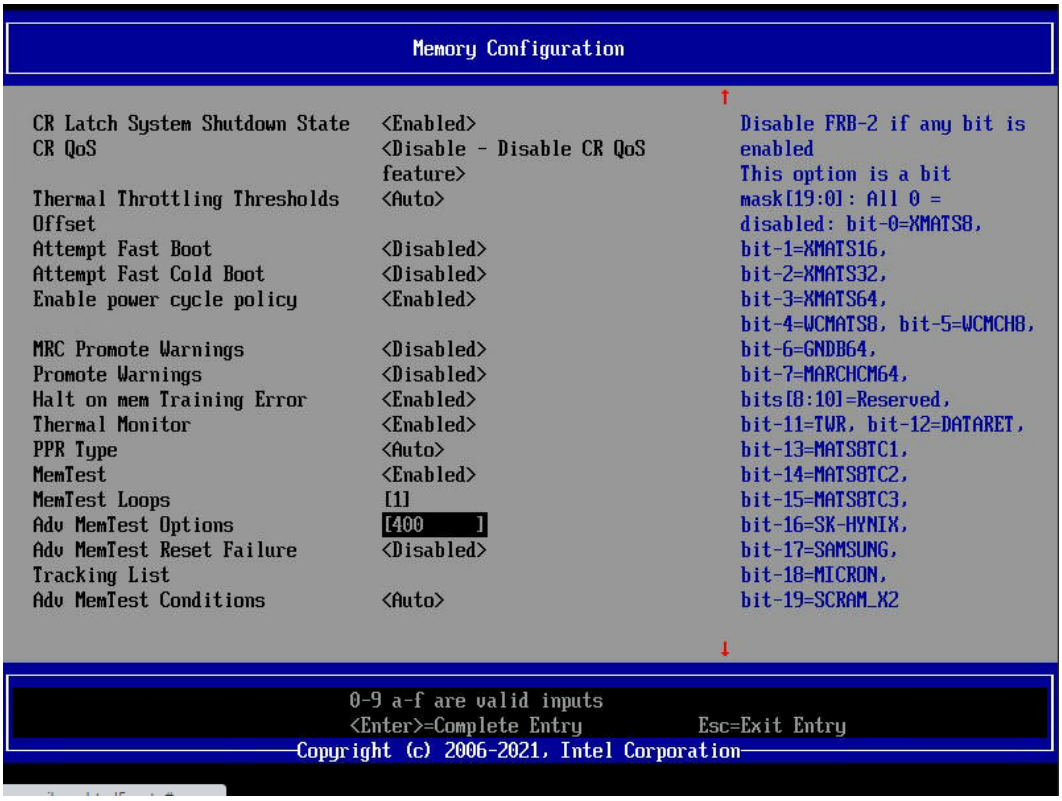
Intel Integrator Toolkit version 5.1.02 and earlier use decimal when editing a BIOS.CAP file. Versions 5.1.03 and later use hexadecimal.

The full table is available in *Advanced MemTest Application in the Server BIOS Memory Reference Code*. See Table 4-1.

Go to Advanced > Memory Configuration > **Adv MemTest Options [ ]**

- Choose memory DIMM vendor: SK Hynix*, Samsung, or Micron*.

If using another vendor, use **[400]** in hexadecimal for bit 10 (RANGE_TEST_SCRAM).



6. POST Package Repair Options

Hard PPR is intended for field applications and end customer installations in data centers. DDR4 memory is required to have at least one spare row per bank group for use with PPR.

Soft PPR is only intended for use in the lab, to test RAS features without permanently fusing memory cells.

7. How to Monitor AMT Activity

System boot time is usually 1–2 minutes without running AMT. The boot time increases about 5 minutes per loop with AMT.

7.1 During BIOS POST

When AMT is inactive, the BIOS POST codes show small groups of:

- **0xB0**–Detect DIMM population.

And quick iterations of:

- **0xB7**–Train DDR4 ranks.

The exact number depends on DIMM population. If the timestamps on the "Train DDR4 ranks" entries are within 0.01 seconds of each other, the BIOS is only reading existing training data, rather than doing a full retrain. The BIOS fully retrains memory:

1. After a complete power cycle.
2. If Attempt Fast Boot and Attempt Fast Cold Boot are [Disabled].
3. If it has been more than 90 days since the last memory training.

When AMT is active, the BIOS POST codes show additional iterations of:

- **0xB0**–Detect DIMM population

And repeated iterations of:

- **0xB7**–Train DDR4 ranks
- **0xB0**–Detect DIMM population
- **0xB9**–Hardware memory test and initialization
- **0xB1**–Set DDR4 frequency

When AMT completes all test loops, the POST code changes to:

- **0xBF**–MRC is done

When all loops are completed. For example, when running MemTest Loops [3], this occurs around the 10–15-minute mark.

The POST codes can be reviewed in the Integrated BMC Web Console under the Server Diagnostics tab:

More details can be found in the corresponding Integrated BMC Web Console user guide.

7.1.1 AMT POST Codes Example

Active AMT

00:01.600	**0xB0**	Detect DIMM population
00:01.600	**0xB0**	Detect DIMM population
00:01.620	**0xB0**	Detect DIMM population
00:01.620	**0xB0**	Detect DIMM population
00:01.620	**0xB0**	Detect DIMM population
00:01.620	**0xB0**	Detect DIMM population
00:01.620	**0xB0**	Detect DIMM population
00:01.630	**0xB0**	Detect DIMM population
00:01.660	**0xB0**	Detect DIMM population
00:01.700	**0xB0**	Detect DIMM population
00:01.700	**0xB0**	Detect DIMM population
00:01.700	**0xB0**	Detect DIMM population
00:01.700	**0xB0**	Detect DIMM population
00:01.700	**0xB0**	Detect DIMM population
00:01.740	**0xB0**	Detect DIMM population
00:01.770	**0xB0**	Detect DIMM population
00:01.780	**0xB0**	Detect DIMM population

00:02.670	**0xB1**	Set DDR4 frequency
00:02.670	**0xB1**	Set DDR4 frequency
00:02.670	**0xB1**	Set DDR4 frequency
00:02.670	**0xB1**	Set DDR4 frequency
00:02.670	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency
00:02.680	**0xB1**	Set DDR4 frequency

00:03.000	**0xB7**	Train DDR4 ranks
00:03.000	**0xB7**	Train DDR4 ranks
00:03.010	**0xB7**	Train DDR4 ranks
00:03.020	**0xB7**	Train DDR4 ranks
00:03.020	**0xB7**	Train DDR4 ranks
00:03.030	**0xB7**	Train DDR4 ranks
00:03.040	**0xB7**	Train DDR4 ranks
00:03.040	**0xB7**	Train DDR4 ranks
00:03.040	**0xB7**	Train DDR4 ranks
00:03.040	**0xB7**	Train DDR4 ranks
00:03.040	**0xB7**	Train DDR4 ranks
00:03.040	**0xB7**	Train DDR4 ranks
00:03.040	**0xB7**	Train DDR4 ranks
00:03.040	**0xB7**	Train DDR4 ranks
00:03.710	**0xB7**	Train DDR4 ranks
00:03.710	**0xB7**	Train DDR4 ranks
00:03.710	**0xB7**	Train DDR4 ranks
00:03.710	**0xB7**	Train DDR4 ranks
00:03.710	**0xB7**	Train DDR4 ranks
00:03.710	**0xB7**	Train DDR4 ranks
00:03.720	**0xB7**	Train DDR4 ranks
00:03.730	**0xB7**	Train DDR4 ranks
00:03.740	**0xB7**	Train DDR4 ranks
00:03.750	**0xB7**	Train DDR4 ranks
00:03.750	**0xB7**	Train DDR4 ranks
00:03.750	**0xB7**	Train DDR4 ranks
00:03.770	**0xB7**	Train DDR4 ranks
00:03.770	**0xB7**	Train DDR4 ranks
00:03.770	**0xB7**	Train DDR4 ranks
00:03.770	**0xB7**	Train DDR4 ranks
00:03.790	**0xB7**	Train DDR4 ranks
00:03.800	**0xB7**	Train DDR4 ranks
00:03.800	**0xB7**	Train DDR4 ranks
00:03.820	**0xB7**	Train DDR4 ranks
00:03.830	**0xB7**	Train DDR4 ranks
00:03.830	**0xB7**	Train DDR4 ranks
00:03.830	**0xB7**	Train DDR4 ranks
00:03.840	**0xB7**	Train DDR4 ranks

00:08.980	**0xB9**	Hardware memory test and init
00:08.980	**0xB1**	Set DDR4 frequency
00:09.000	**0xB9**	Hardware memory test and init
00:16.770	**0xB9**	Hardware memory test and init
00:24.060	**0xB9**	Hardware memory test and init

00:32.750	**0xBF**	MRC is done

7.2 Review AMT Log Entries in the SEL

After POST has completed, AMT and PPR activity is logged in the SEL. The SEL shows whether the BIOS is functioning normally. If the BIOS is functioning as it should, it will keep the DIMMs healthy.

If the SEL shows:
Advanced Memory Test Error
followed by:
POST Package Repair Finish
then the row read failed more than once. PPR has since repaired the issue, and no further action is required.

If the SEL shows:
Advanced Memory Test Completion with Error
or
POST Package Repair Failure
replace the listed DIMM.

If the SEL shows:
Correctable ECC
and performance is not impacted, then no further action is required. The error was already corrected.

If the SEL shows:
Correctable ECC
and the system is becoming sluggish; reboot, enable AMT, select your memory vendor, and run AMT.

If the SEL shows:
Uncorrectable ECC error
rebooting will automatically run PPR. PPR should resolve the issue, and no further action would be required.

Important Notice

For BIOS revisions 02.01.0014 and 22.01.0097:

1. If a runtime PPR request occurs, an SEL entry log is generated and displayed. The BIOS may repair the error, but no event will be logged in the SEL (i.e., no "successfully repaired" is entered). Only the PPR request is logged in the SEL.
2. If during boot time an AMT test failure occurs, the BIOS memory code tries with a PPR repair. If the attempt is successful, a memory code is created and then a PPR repair event is triggered in the SEL.

In BIOS revisions **02.01.0015** and **22.01.0098**, Intel enhanced the memory code to record the PPR repair finish event in log for the runtime PPR request. These are normal BIOS POST codes:

- SEL logs with generator ID (GID) 0x01.
- Sensor Type (ST) 0x0F.
- ED1 (E1) of 0xA0.

AMT and PPR execution add additional entries to the SEL as detailed in Table 7-1. **Read the previous Important Notice for BIOS versions enhancements.**

7.2.1 LOG Entries

SEL logs with GID 0x01, ST 0x0F or 0x12, and ED1 of 0xA1, 0xA2, 0xA3, 0x04, 0x05, 0xA4, or 0xA5 are new POST codes added for AMT and PPR logging.

A preceding 'A' in ED1 signifies relevant data in ED2 and ED3. If the first nibble in ED1 is 0, then the data in ED2 and ED3 is unspecified or meaningless. See the Table 29 (Event Request Message Event Data Field Contents | OEM) of the IPMI specifications (version 2, revision 1) for more details.

SEL logs with GID 0x33, ST 0x0C, and ED 0x01 or 0x02, indicate that an error during runtime has triggered a request for PPR on the next boot.

`04h = Advanced Memory Test Completion without Error` may be logged whether AMT is enabled or disabled. This entry can be ignored. This SEL entry may be removed in a future version.

Table 7-1 SEL Entries

Sensor Name	Sensor Number	Sensor Owner (GID)	Sensor Type	Event/Reading Type Offset Values	Event Data 2 Event Data 3
BIOS POST Error	06h	01h (BIOS POST)	0Fh (System Firmware Progress)	6Fh (Sensor Specific Offset) A1h = Advanced Memory Test Error A2h = POST Package Repair Finish A3h = POST Package Repair Failure	ED2 = [7:4] = DIMM index 0–1= DIMM 1–2, DIMM index per channel [3:0] = Rank index Physical rank index per DIMM ED3 = [7:4] = Socket index 0–3= CPU1-4 [3:0] = Channel index 0–5 = Channel A-F, Channel index for Socket
OEM BIOS POST Event	10h	01h (BIOS POST)	12h (System Event)	7Fh (OEM Discrete) ~~04h = Advanced Memory Test Completion without Error~~ A5h = Advanced Memory Test Completion with Error	
Memory Error Extension	10h	33h (SMI Handler)	0Ch (Memory)	7Fh (OEM Discrete) A1h = POST Package Repair Runtime Request A2h = POST Package Repair Runtime Request Failure–queue limit reached	

In these SEL entries (see Table 7-1):

- **1h = Advanced Memory Test Error**–Indicates that a row has failed a read more than once.
- **5h = Advanced Memory Test Completion with Error**–Indicates that AMT triggered a PPR action, and further data errors were found after PPR.
- **3h = POST Package Repair Failure**–May occur if no spare rows are available.
- **04h = Advanced Memory Test Completion without Error**–May be logged whether AMT is enabled or disabled. This entry can be ignored. This SEL entry may be removed in a future version.

Table 7-2 Event Data 2 (ED2) Detail

ED2	DIMM	RANK
0x00	DIMM 1	Rank 0
0x01	DIMM 1	Rank 1
0x02	DIMM 1	Rank 2
0x03	DIMM 1	Rank 3
0x10	DIMM 2	Rank 0
0x11	DIMM 2	Rank 1
0x12	DIMM 2	Rank 2
0x13	DIMM 2	Rank 3

Table 7-3 Event Data 3 (ED3) Detail

ED3	CPU	Memory Channel
0x00	CPU1	Channel A
0x01	CPU1	Channel B
0x02	CPU1	Channel C
0x03	CPU1	Channel D
0x04	CPU1	Channel E
0x05	CPU1	Channel F
0x10	CPU2	Channel A
0x11	CPU2	Channel B
0x12	CPU2	Channel C
0x13	CPU2	Channel D
0x14	CPU2	Channel E
0x15	CPU2	Channel F
0x20	CPU3	Channel A
0x21	CPU3	Channel B
0x22	CPU3	Channel C
0x23	CPU3	Channel D
0x24	CPU3	Channel E
0x25	CPU3	Channel F
0x30	CPU4	Channel A
0x31	CPU4	Channel B
0x32	CPU4	Channel C
0x33	CPU4	Channel D
0x34	CPU4	Channel E
0x35	CPU4	Channel F

7.2.2 SEL Examples

7.2.2.1 PPR Fail

```
EventID:0032
Time:Fri Jan 1 00:11:55 2016
Controller:BIOS
SensorType:System Firmware Progress
SensorName:POST Err Sensor
Description:POST Package Repair Failure Rank: 0 CPU: 1 DIMM: A1. – Asserted
RID:0032 RT:02 TS:5685C44B GID:0001 ER:04 ST:0F S#:06 ET:6F ED:A3 00 00
EXT:01 FF FF FF FF FF FF FF
```

7.2.2.2 AMT Fail and PPR Finish

```
EventID:0129
Time:Wed Jan 1 00:13:55 2020
Controller:BIOS
SensorType:System Firmware Progress
SensorName:POST Err Sensor
Description:Advanced Memory Test Failure Rank: 1 CPU: 2 DIMM: E1. – Asserted
RID:0129 RT:02 TS:5E0BE443 GID:0001 ER:04 ST:0F S#:06 ET:6F ED:A1 01 14
EXT:01 FF FF FF FF FF FF FF
EventID:0130
Time:Wed Jan 1 00:13:55 2020
Controller:BIOS
SensorType:System Firmware Progress
SensorName:POST Err Sensor
Description:POST Package Repair Finish Rank: 1 CPU: 2 DIMM: E1. – Asserted
RID:0130 RT:02 TS:5E0BE443 GID:0001 ER:04 ST:0F S#:06 ET:6F ED:A2 01 14
EXT:01 FF FF FF FF FF FF FF
```

7.2.2.3 POST Package Repair Runtime Request

```
01/04/2020-01:11:23 POST Package Repair Runtime Request
RID:0100 RT:02 TS:52E60F5E GID:0033 ER:04 ST:0C S#:10 ET:7F ED:A1 00 04
EXT:01 FF FF FF FF FF FF FF
```

Appendix A. FAQs

A.1 Memory Error Correction Code

What is a Memory Error Correction Code (ECC)?

ECCs for correctable errors represent a threshold overflow for a given Dual In-line Memory Module (DIMM) within a given time frame.

The ECC errors are self-correcting. Depending on the reliability, availability, serviceability (RAS) configuration of the memory, the integrated memory controller (IMC) may take the affected DIMM offline.

For different Intel server platforms, there are some differences in their event definition. Refer to the *System Event Log Troubleshooting Guide* for your server platform.

Intel recommends downloading and updating the system BIOS to the latest available version for your server platform.

A.2 Responding to an ECC

How do Intel® Server Systems respond to an ECC?

Memory errors are processed in system management mode (SMM) by the SMI handler. ECCs for uncorrectable errors (UCE) are fatal unless the system is running in mirrored mode. The SMI handler attempts to log the error, and pass control on to the operating system error handlers, before the terminating operations.

Correctable errors (CEs) ECCs are counted, and when a certain threshold value is reached, a CE event occurs. This event is handled by the SMI handler, much like an UCE, except it is not fatal and execution continues unless the operating system error handlers terminate execution.

When an ECC for a CE or UCE event is generated, it is logged via the BMC SEL.

For Intel® Xeon® Scalable processors H0 in ADDDC/SVL mode, once the per-rank counter reaches the threshold and the SMI is triggered, the BIOS programs the threshold for the per-rank CE counter to half of the normal value b/c.

Appendix B. Glossary

Acronym	Description
ADDDC	Adaptive Double Device Data Correction
AMT	Advanced Memory Test
BIOS	Basic Input/Output System
BMC	Baseboard Management Controller
CE	Correctable Error
DDR	Double Data Rate
DIMM	Dual in-line Memory Module
DRAM	Dynamic Random Access Memory
DSG	Datacenter Solutions Group
ECC	Error Correctable Code
FRB-2	Fault Resistant Booting Level 2
GID	Generator ID
IMC	Integrated Memory Controller
IPMI	Intelligent Platform Management Interface
ITK	Intel Integrator Toolkit
MRC	Memory Reference Code
MT/s	Mega Transfers per second, a measurement of bus and channel speed in millions of "effective" cycles per second.
OEM	Original Equipment Manufacturer
PEF	Platform Event Filter
PFR	Platform Firmware Resilience
POST	Power-On Self-Test
PPR	POST Package Repair
RAS	Reliability Availability Serviceability
SEL	System Event Log
SMI	System Management Interface
SMM	System Management Mode
SMNP	Simple Network Management Protocol
UCE	Uncorrectable Error
URI	Uniform Resource Identifier